Ciencias Físicas: Especialidad de Física Industrial
ELECTRÓNICA II (cód. 075098) MÓDULO VI

TEMA 36

CONVERSORES A/D

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1. Introducción

En la figura 1 repetimos el esquema general del procesado digital de señales analógias que usamos en el tema anterior para introducir los conversores D/A. Allí comentábamos que estudiaríamos primero la conversión D/A porque era más sencilla y porque en algunos casos el conversor D/A se usaba como bloque funcional en el diseño de conversores analógico-digitales (A/D). Ahora ya podemos estudiar estos conversores A/D que aparecen a la entrada de todo procesador digital. En el camino natural de la señal, primero está la conversión de estas señales (audio, imágenes, etc...) en una representación digital (conversión A/D), después el procesado digital y, finalmente, la conversión D/A, que ya hemos estudiado.

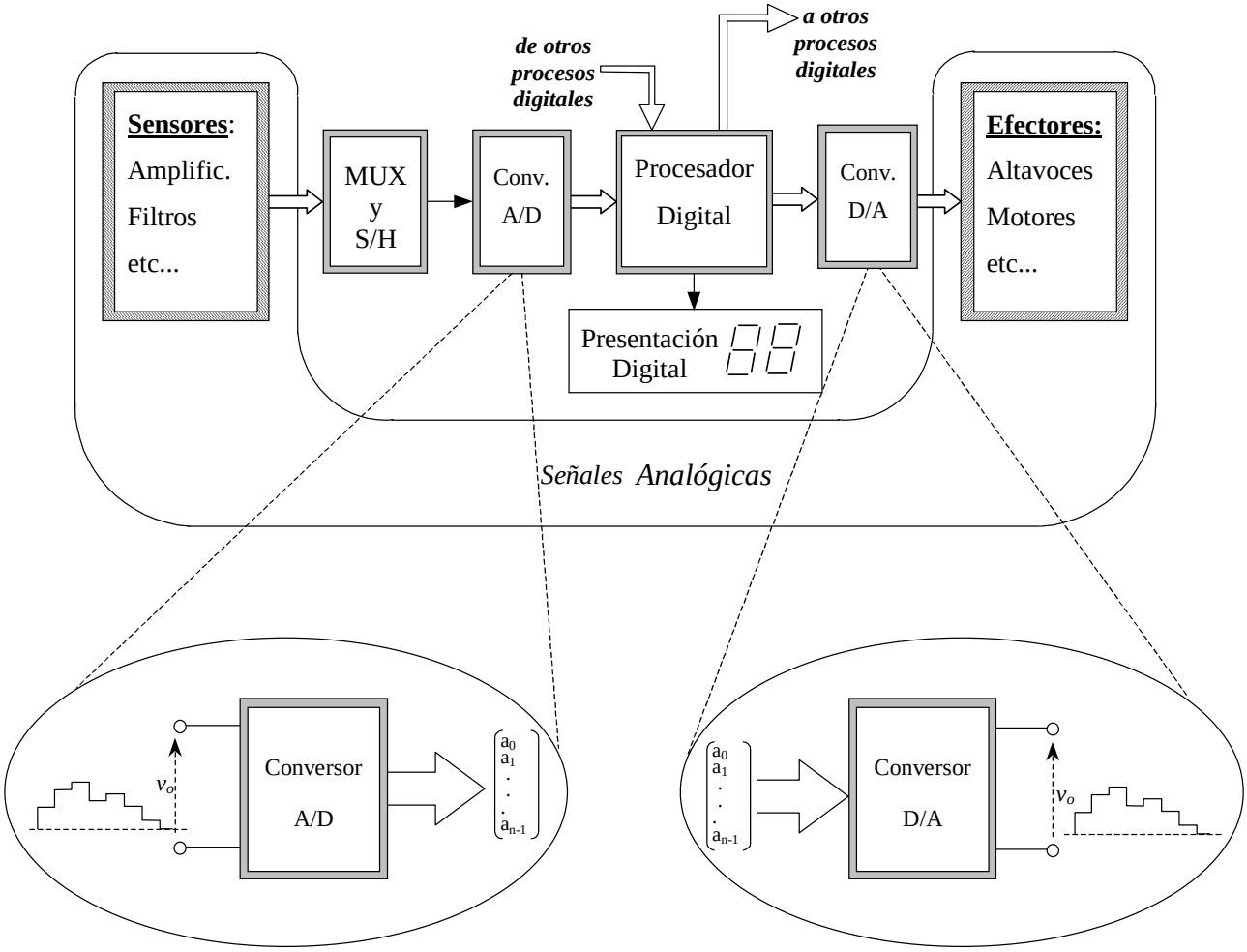


Fig. 1. Repetición del esquema general del tratamiento digital de señales analógicas con las posiciones de los conversores A/D y D/A y los cambios inversos que realizan en la representación de la información. El conversor A/D pasa de la señal analógica escalonada a la palabra binaria (a_0, . . . , a_{N-1}).

Un conversor A/D es un circuito electrónico que acepta como entrada la salida de un circuito de muestreo-retención cuantificada en 2N escalones y produce como salida una representación digital (binaria) de N bits presentada, en general, a través de N líneas en paralelo. Hay muchos tipos de conversores A/D integrados y su selección depende de un conjunto de criterios tales como:

(1) Precisión necesaria en la aplicación en la que se va a integrar ese conversor.

(2) Resolución (número de bits) necesario.

(3) Naturaleza de la señal analógica que queremos convertir en digital.

(4) Velocidad de conversión.

(5) Carácter general o "especial" (condiciones ambientales rigurosas, tipo de arquitectura interna, etc...).

En una primera aproximación, el alumno puede empezar a crearse su visión de los conversores A/D pensando sólo en términos de dos criterios conflictivos: ***precisión*** y ***velocidad***. Estos parámetros representan las dos grandes áreas de aplicación: la ***instrumentación de medida*** (baja frecuencia) y **las *señales de amplio espectro*** (vídeo). En la instrumentación, la señal analógica a convertir varía lentamente y por eso la meta es la precisión. En el tratamiento digital de señales de amplio espectro, el teorema del muestreo de Shannon pone una cota mínima a la velocidad de conversión, si queremos mantener la información tras el proceso de muestreo, retención y conversión.

Sin embargo, al comienzo del tema nos centraremos, por razones pedagógicas, en los principios generales (los "algoritmos" o métodos) en los que se basa el proceso de conversión A/D. En primera aproximación, podemos clasificar todos estos métodos de conversión atendiendo a los siguientes criterios:

- ✧ ***Programados*** o ***no programados***
- ✧ ***De lazo abierto*** o ***realimentados*** (lazo cerrado)

En los ***programados***, la conversión se hace en un número dado de etapas sea cual fuese el valor de la muestra a convertir. Es decir, el proceso de conversión dura un cierto número fijo de intervalos de reloj. En los ***no programados*** (asíncronos), la conversión no se realiza en tiempo fijo, sino siguiendo una determinada secuencia de sucesos que consumen un intervalo de tiempo mayor o menor dependiendo del valor de la muestra.

En los algoritmos de conversión en ***lazo abierto*** se compara la muestra con un conjunto de señales de referencia. Como resultado de la comparación se genera directamente una palabra digital equivalente a la señal analógica.

En los esquemas en ***lazo cerrado*** se genera una secuencia de palabras que se convierten en señal analógica (con un conversor D/A) y se comparan con la muestra que se está convirtiendo. Cuando ambas coinciden se detiene el proceso y se saca la palabra digital correspondiente.

Dentro de cada uno de estos métodos generales existe a su vez una gran variedad de soluciones, aunque sólo algunas de estas se han mostrado adecuadas para su realización en tecnología integrada. Por ejemplo, en ***lazo abierto*** se puede usar:

- ✧ ***Conversión Tensión-frecuencia***
- ✧ ***Modulación en anchura de impulsos***
- ✧ ***Conversión Simultánea*** (paralelo)

Y dentro de las técnicas en ***lazo cerrado***, podemos señalar las siguientes variedades:

- ✧ Métodos ***integradores***, en los que se carga o descarga un condensador durante el ciclo de conversión.
- ✧ Métodos típo "***rampa y contador***" en los que se usa un contador binario y un conversor D/A en el lazo de control.
- ✧ Métodos de ***Aproximaciones sucesivas***, que producen una señal digital de salida por pasos sucesivos de prueba y error.
- ✧ Métodos ***híbridos***, que combinan dos o más técnicas (por ejemplo, paralelo con aproximaciones sucesivas).

Por razones pedagógicas, al igual que en el tema anterior, estudiaremos primero la caracterización funcional, después los distintos métodos de conversión y, finalmente, la caracterización como elemento de circuito y los datos de catálogo de circuitos reales representativos.

2. Caracterización de la Conversión A/D

Teóricamente, la función de transferencia de un conversor A/D ***ideal*** es una línea recta. Sin embargo, en la práctica, esa función de transferencia ideal es una ***escalera*** uniforme, con todos los escalones iguales, tal como se ilustra en la figura 2, consecuencia del carácter discreto y cuantificado de su respuesta. Ante una señal analógica continua en un cierto rango, la respuesta de un conversor de N bits está cuantificada en 2^N niveles (8 para 3 bits, 16 para 4 bits, etc.). Cada configuración de esos N bits representa una fracción del rango total de la señal analógica, pero siempre habrá un error. Lógicamente, al aumentar el número de bits (la precisión del conversor) disminuye el error porque hay más escalones (el doble por cada nuevo bit) y estos son más pequeños.

El ancho de un escalón se define como el bit menos significtivo (LSB) y se usa como unidad de referencia para otras magnitudes necesarias en la especificación de las características de un conversor. Obviamente, también es una medida de la resolución del conversor, puesto que define el número de unidades que caben dentro de todo al rango dinámico de la variable analógica.

La resolución se expresa en general en términos del número de bits, N, de su código digital de salida. Las 2^N configuraciones posibles se asocian con los 2^N escalones. Sin embargo, como el primer escalón y el último son la mitad de anchos que el resto (ver de nuevo la figura 2), el fondo de escala (FSR –"full-scale-range") se divide en 2^N-1 intervalos. Así, para un conversor de N bits el valor del bit menos significativo será,

$$1\,LSB = \frac{FSR\ (total\ del\ \ fondo\ de\ escala\ en\ la\ señal\ analogica)}{2^N - 1}$$

Por ejemplo, para $N=3$, $2^N-1=8-1=7$, de forma que si el fondo de escala es *7 volts*. (para que nos salga sencillo), LSB=1 volt. Si en vez de usar un conversor de sólo tres bits usáramos uno de 8 bits (mayor resolución), tendríamos,

$$1\ LSB = \frac{7}{2^8 - 1} = \frac{7}{256 - 1} = \frac{7}{255} = 0'027\ volts$$

Es decir, aumentar la resolución significa hacer más pequeños los intervalos del rango dinámico de la señal analógica a los que se asigna un código binario de salida. Esta salida

binaria es constante para todos los valores de la señal analógica de entrada en un rango de 1 LSB en torno al valor central.

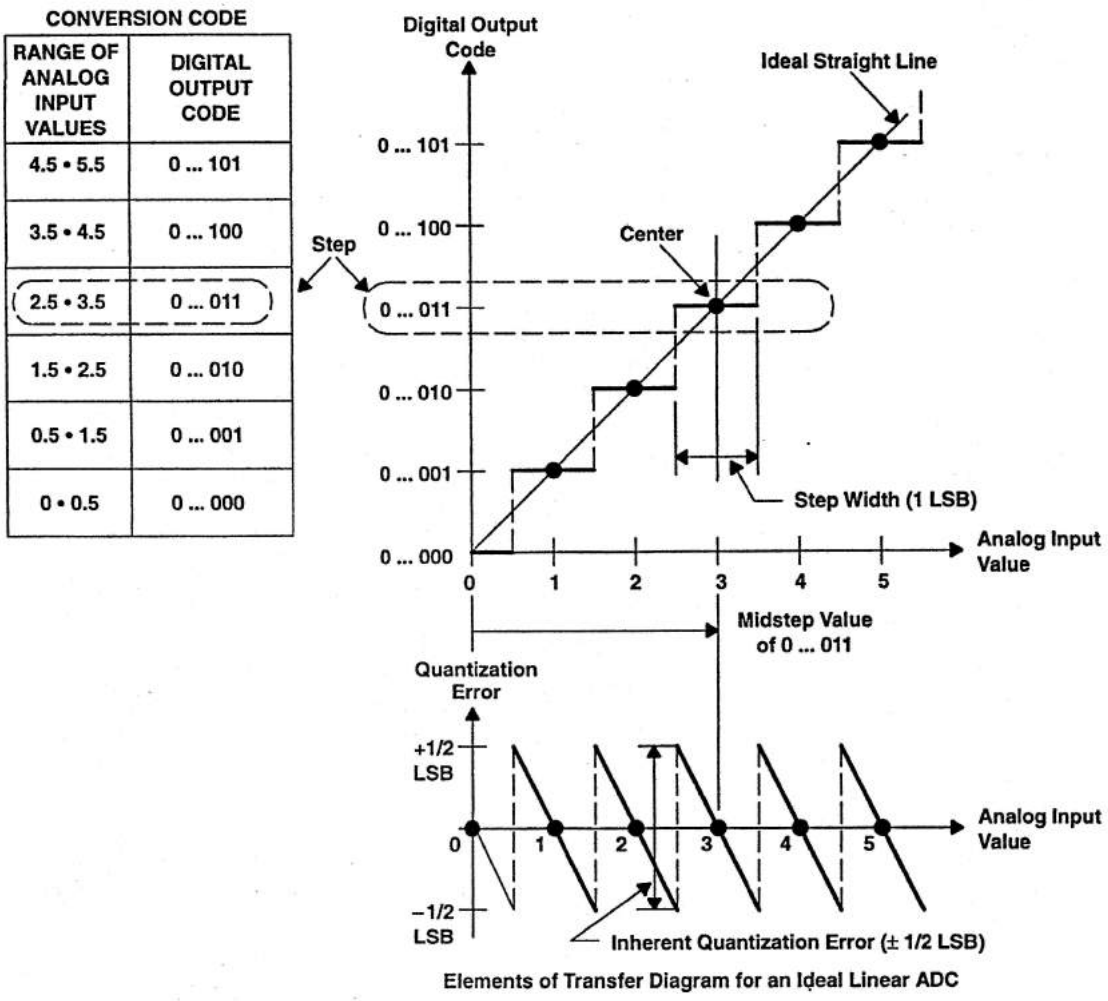


Fig. 2. Función de transferencia ideal de un conversor A/D. Obsérvese como se distribuye todo el rango dinámico de la variable analógica (eje de abscisas) en los 2^N escalones correspondientes a las 2^N configuraciones mutuamente exclusivas del código digital (eje de ordenadas). La señal triangular de la parte inferior muestra la forma del error de cuantificación, que es nulo para los valores que coinciden con el escalón y aumenta, entre escalones, siendo máximo e igual a ***½LSB*** en el punto medio entre peldaños[1]**.**

Las características que definen a un conversor A/D están asociadas a la minimización de los errores que, apartan su característica de transferencia real de la ideal. Veamos estas fuentes de error.

Son errores estáticos aquellos que afectan la precisión del conversor cuando está convirtiendo una señal analógica continua, y se pueden agrupar en cuatro términos:

[1] Estas figuras están tomadas de una nota de aplicación de Texas Instruments, a través de la red (www.ti.com)

- ✧ ***Error de offset***
- ✧ ***Error de ganancia***
- ✧ ***Error de no linealidad integral***.
- ✧ ***Error de no linealidad diferencial***

Todos ellos pueden expresarse en unidades LSB o en porcentajes del fondo de escala. Por ejemplo, un error de ½ LSB en un conversor de 8 bits corresponde al 0'2% del fondo de escala.

La figura 3 muestra el ***error de offset*** que se define como la diferencia entre el valor nominal y el actual del punto de offset. El punto de offset nominal es la mitad del ancho del escalón cuando la salida digital es cero. En la figura se ilustra el caso en el que ese error es de (1'25 LSB). Este error de desplazamiento del origen afecta a todos los códigos de salida de la misma manera y puede compensarse ajustando el circuito. Cuando el ajuste no puede disminuirlo más, al valor residual se le llama ***error del cero de la escala***.

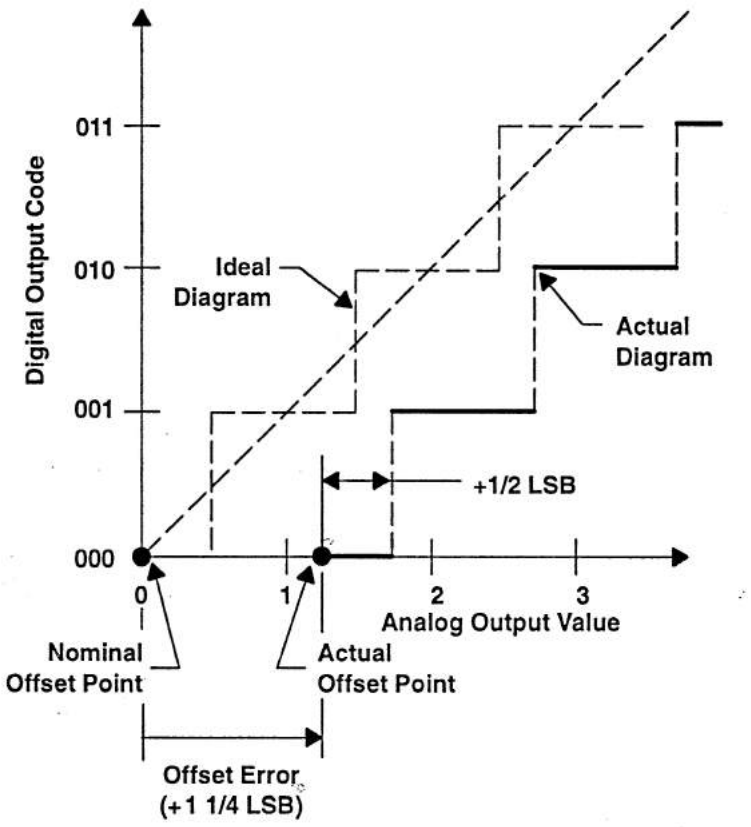


Fig.3. Error de offset de un conversor A/D lineal de 3 bits especificado para el paso (000).

El ***error de ganancia***, tal como se ilustra en la figura 4, se define como la diferencia entre los puntos de ganancia nominal y actual sobre la función de transferencia, una vez que hemos corregido el error de offset. Para un conversor A/D el punto de ganancia es el valor en el punto medio del paso cuando la salida digital es la máxima (111, para un conversor de 3 bits). La figura 4 aclara este concepto. El valor nominal es (111) para 7 volts (máximo del fondo de escala digital asociado al máximo del fondo de escala analógico). Si el valor real es distinto de este, hay un error (-3/4 del LSB en el ejemplo)

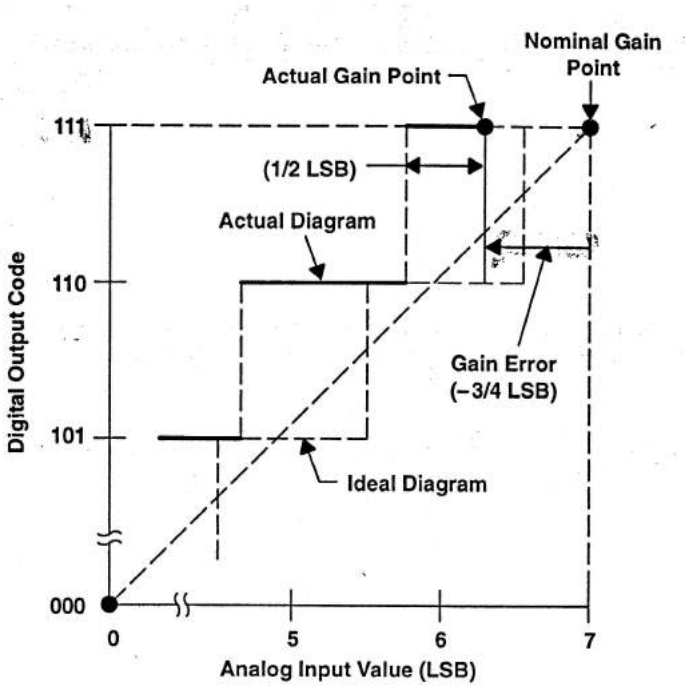


Fig. 4. Error de ganancia para un conversor A/D de 3 bits.

El ***error de no linealidad diferencial*** ("DNL error") se ilustra en la figura 5 y es la diferencia entre los valores reales del ancho de cada uno de los escalones y el valor ideal de 1LSB. Si este error excede el valor de 1LSB, existe la posibilidad de que el proceso de conversión no sea monótono. Es decir, que la magnitud de la salida se haga más pequeña cuando aumente la magnitud de la entrada. Además, nos podemos "saltar" algún código. Es decir, alguna de las 2^N configuraciones binarias de salida puede no aparecer nunca, pasando de la anterior a la siguiente.

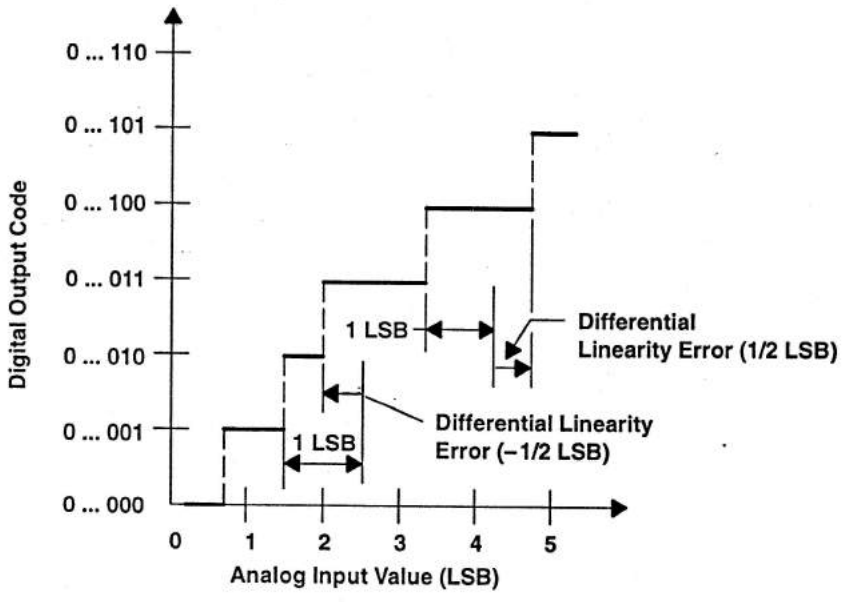


Fig.5. Error diferencial de linealidad en un conversor A/D.

El ***error integral de no linealidad*** ("INL error") se muestra en la figura 6 y se define como la desviación de los valores actuales de la función de transferencia del conversor A/D, de la línea recta. Esta recta se suele trazar entre los puntos inicial (000) y final (111), una vez que se han compensado los errores de offset. En este caso se le llama "linealidad entre puntos extremos" (end-point linearity").

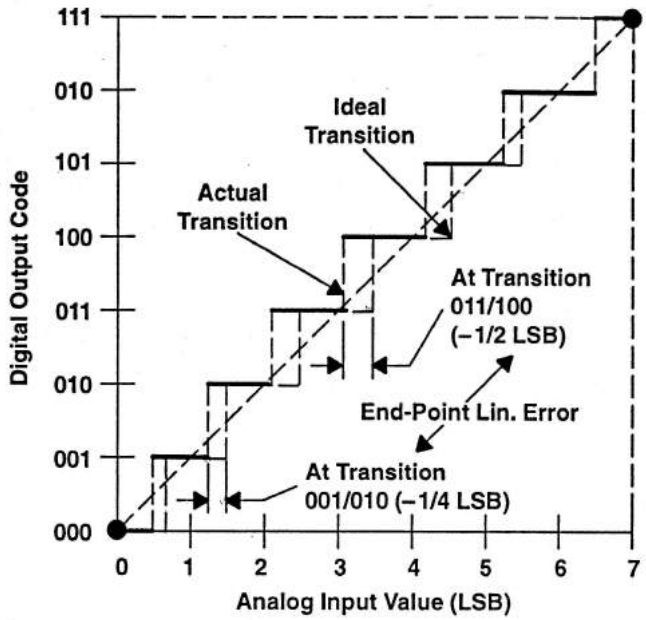


Fig. 6. Error de no linealidad integral.

El ***valor absoluto del error*** es el valor máximo de la diferencia entre un valor analógico y el valor ideal correspondiente en el punto central del escalón. Se ilustra en la figura 7 e incluye ***offet***, ***ganancia***, ***linealidad*** y ***cuantificación***.

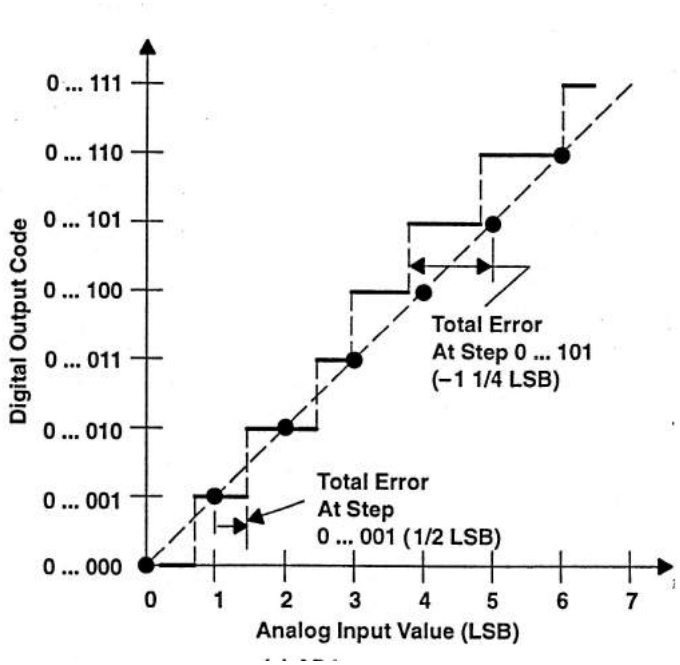


Fig. 7. Error absoluto

Conocemos el significado de todos estos errores, salvo el debido al proceso de cuantificación, que es el más obvio ya que se debe al carácter continuo de la señal analógica de entrada y al carácter discreto (sólo 2^N valores) de la señal digital de salida. Ya comentamos al comienzo del tema que la resolución del conversor era función del número de bits pero sea cual fuese este número, siempre tendríamos una señal en escalera en respuesta a una señal continua, con lo que varios valores de la señal analógica se tendrán que englobar en un único código digital. Este es el origen del error de cuantificación, tal como se ilustra en la figura 8.

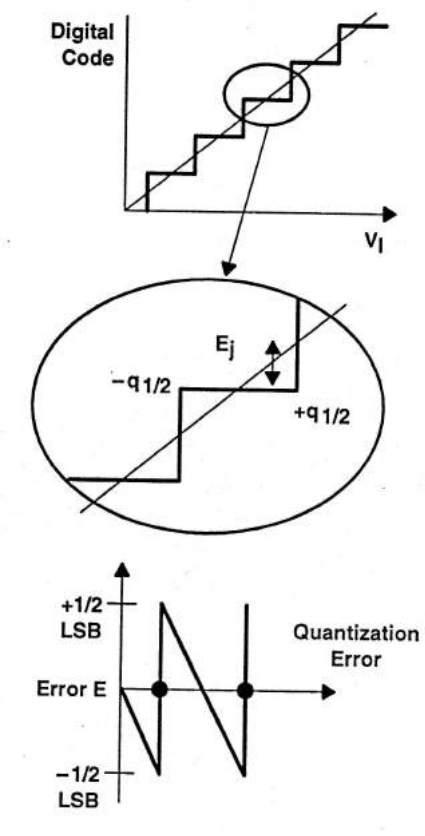


Fig.8. Forma triangular del error de cuantificación que oscila entre +1/2LSB y –1/2LSB, siendo nulo sólo para el valor analógico que corresponde al centro de cada escalón.

El panorama global de los posibles errores asociados a un conversor A/D se completa con los errores de ***apertura*** y de ***muestreo***. El primero está asociado a la incertidumbre en el tiempo en el cual el circuito de ***muestreo-retención*** que precede a todo A/D va a pasar del modo "muestrear" al modo "retener". El segundo está asociado con el ***teorema de Shannon*** sobre la frecuencia mínima de muestreo necesaria para poder recuperar la señal original a partir de sus muestras, sin pérdida de información. Aquí, no nos vamos a extender en este punto porque ya fue considerado en el tema 34 al hablar de multiplexos. Recordemos sin embargo, que su origen estaba en el carácter de "no limitadas en banda" de todas las señales reales y la necesidad de eliminar la mezcla de las componentes de alta frecuencia no deseadas con las de baja ("aliasing") en las fronteras del corte pasa-baja del filtro de recuperación del espectro original[2].

[2] Hay filtros Butterworth "antialiasing", tipo TLC04, que preceden al conversor A/D para minimizar el efecto de mezcla de espectros.

Volveremos a la caracterización de conversores y a los criterios de selección en función de la aplicación al final del tema, cuando conectemos con los ***datos de catálogo***. Ahora vamos a considerar aspectos más académicos del proceso de conversión A/D estudiando un conjunto de métodos básicos de conversión.

3. Métodos de Conversión en Lazo Abierto

Como hemos dicho en el apartado anterior los ***métodos de conversión en lazo abierto*** que vamos a estudiar son:

- ✧ ***Conversión tensión-frecuencia***
- ✧ ***Modulación en anchura de impulsos***
- ✧ ***Conversión simultanea (paralelo)***

3.1 Conversión tensión-frecuencia

El esquema de un conversor A/D que utiliza como base la conversión tensión-frecuencia se muestra en la figura 9. La señal analógica, V_A, entra al circuito de muestreo-retención que genera la señal de entrada al convertidor tensión-frecuencia. Este bloque funcional produce una señal de salida cuya frecuencia es proporcional al nivel de tensión de entrada, de forma que en su salida obtenemos una señal modulada en frecuencia. Si la forma de esta señal modulada en frecuencia es sinusoidad o cuadrada puede ser necesario añadir un circuito de conformación de ondas, tipo monoestable o disparador de Schmith por ejemplo, que nos produce un tren de impulsos.

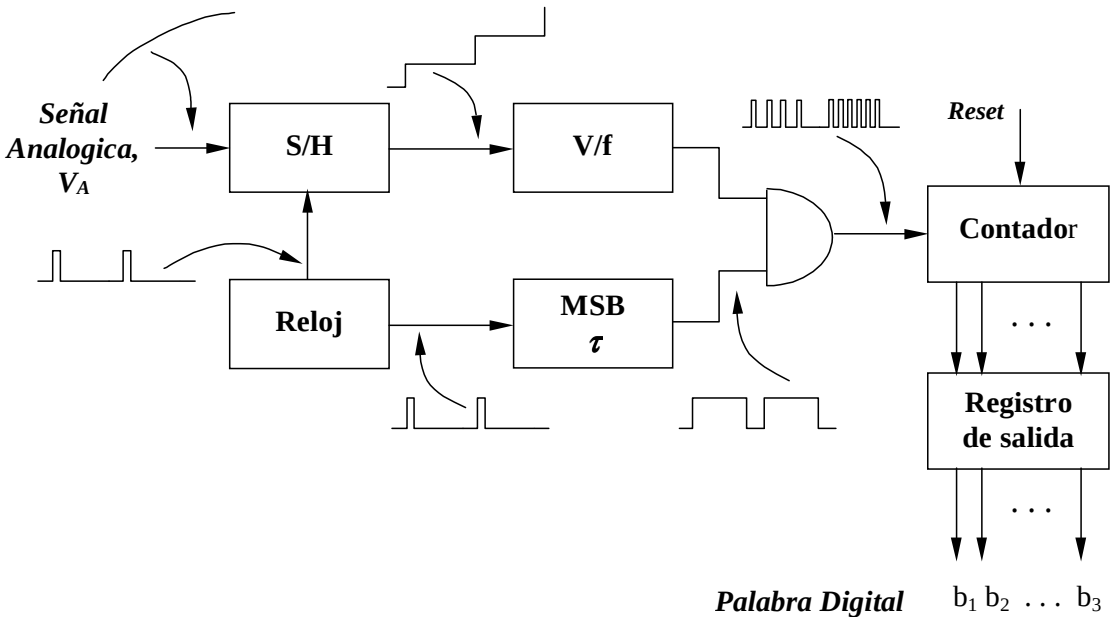


Fig. 9. Diagrama de bloques de un conversor A/D por el método de convertidor tensión-frecuencia

Existe un reloj general del sistema que controla al S/H y a su vez dispara a un monoestable que genera pulsos de duración τ, algo inferior al período de muestreo (periodo del reloj). Los pulsos generados por el monoestable actúan como señal de control de un

conmutador analógico o de una puerta lógica, de forma que sólo pasan al contador los pulsos procedentes del convertidor V/f durante un tiempo constante y preciso, τ. Dado que la frecuencia de los pulsos es proporcional al valor de la muestra, también lo será el número de los pulsos que se han generado en τ. Así, basta ahora contar estos pulsos para obtener la representación digital de la muestra, V_A.

Al final de la conversión, el contenido del contador debe pasar a un registro de salida donde permanecerá hasta la llegada de la muestra siguiente, permitiéndonos así poner a cero al contador y repetir el proceso. Obsérvese que hay que ajustar el número de bits (N) al rango de la señal analógica, $2^N \geq V_A(max)$ y al factor de proporcionalidad en el conversor tensión-frecuencia. Las limitaciones de esta técnica se deben a las no linealidades del conversos V/f y a la precisión del pulso de duración τ.

3.2. Modulación en anchura de impulsos

Otro tipo de conversor A/D, en lazo abierto, es el que usa la solución complementaria a la anterior. Es decir, se deja fija la frecuencia del oscilador y se utilizan las muestras para modular en anchura un tren de impulsos que actúan como señal de control de un conmutador analógico o una puerta lógica. El efecto final es el mismo, ya que al contador entran un número de pulsos proporcional al valor de la muestra. La figura 10 muestra el diagrama de bloques de este tipo de circuito, que se conocen con el nombre de ***convertidores A/D de integración***. También se llaman ***indirectos*** o de ***modulación en anchura de pulsos***. Ahora la señal analógica de entrada se convierte a un pulso de duración proporcional a dicha señal analógica. Esta duración del pulso se mide de forma digital, contando el número de ciclos del reloj (de frecuencia estable) que caben dentro del pulso generado por la señal de entrada, obteniéndose a la salida una palabra digital (b_1, b_2, ..., b_3) correspondiente al número de pulsos que le ha entrado al contador.

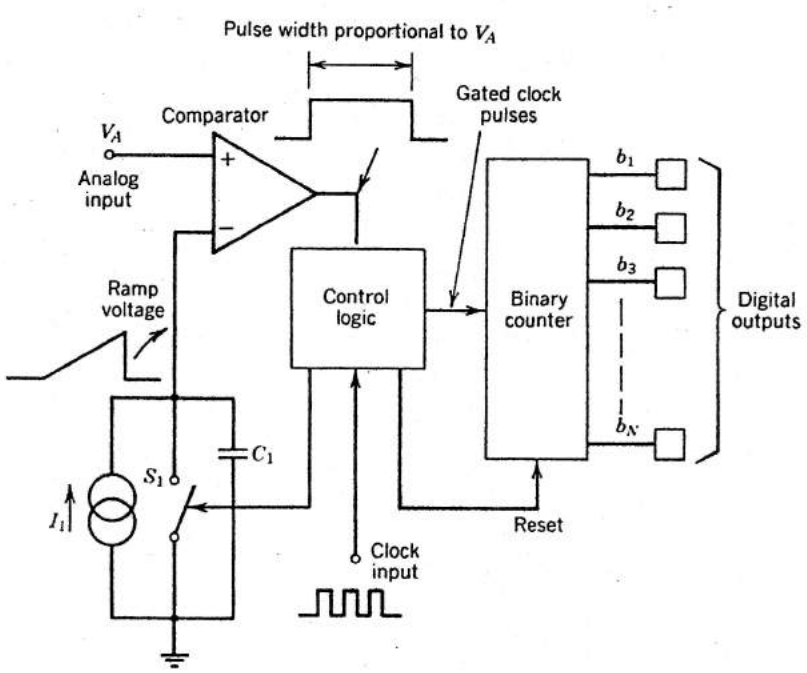


Fig. 10. Diagrama de bloques de un convertidor A/D de integración

Antes de comenzar el ciclo de conversión, el contador se pone a cero y el conmutador S_1 estará cerrado. Cuando empieza el ciclo de conversión, se abre el conmutador S_1 y el

condensador C_1empieza a cargarse de forma lineal a partir del generador de corriente, generando la señal en forma de rampa que se muestra en la figura 10. A la salida del comparador analógico aparece un pulso cuya duración está controlada por el valor de la tensión en bornes del condensador, ya que cuando esta alcance el valor correspondiente a la señal de entrada, $\boldsymbol{V_A}$, la salida del comparador pasará a cero.

Durante todo el tiempo que el condensador ha estado cargándose el contador ha estado contando los pulsos de reloj y con la bajada del pulso que se genera a la salida del comparador se detiene el contador, finalizando así el ciclo de conversión. La cuenta final del contador es el valor digital correspondiente a la señal analógica de entrada, $\boldsymbol{V_A}$. Así. por ejemplo, si suponemos que hacen falta $\boldsymbol{N_T}$ pulsos para que el contador digital alcance el estado binario equivalente a fondo de escala, $\boldsymbol{V_{FS}}$, y el estado del contador es $\boldsymbol{n}$ cuando la salida del comparador pasa a cero y se detiene el contador, se verifica que

$$n = N_T \frac{V_A}{V_{FS}}$$

Para una resolución de $\boldsymbol{N}$ bits, $\boldsymbol{N_T = 2^N}$, y la salida del contador será:

$$n = 2^N \frac{V_A}{V_{FS}}$$

La cantidad acumulada $\boldsymbol{n}$ en el contador es cuantificada en incrementos de unidades de ciclo de reloj. Por tanto, cada ciclo de reloj adicional corresponde a un incremento de 1LSB. Esta cantidad acumulada se visualiza normalmente como el estado digital de un contador binario de $\boldsymbol{N}$ etapas o biestables. Así, la salida de la primera etapa del contador, es decir la que cambia de estado con cada ciclo de reloj, es la correspondiente al LSB y la última etapa que cambia con cada $\boldsymbol{2^{N-1}}$ ciclos de reloj corresponde a la salida MSB.

Este conversor es interesante para entender el principio de funcionamiento, pero en la práctica no se usa debido a la imprecisión asociada al punto de inicio de la rampa, así como al control de los valores absolutos de $\boldsymbol{I_1}$ y $\boldsymbol{C_1}$. Algunas de estas deficiencias se eliminan usando ***métodos de integración en rampa*** y en ***doble rampa.***

Los ***conversores en rampa*** y en ***lazo abierto*** tiene un principio de funcionamiento análogo al visto anteriormente salvo que la tensión de la rampa no empieza exactamente en cero, sino que lo hace en un nivel de tensión ligeramente inferior, es decir en un valor ligeramente negativo.

La figura 11 muestra el diagrama de bloques de este tipo de conversor así como las formas de onda asociadas a los puntos más significativos. Veamos su funcionamiento.

Inicialmente el conmutador $\boldsymbol{S_1}$ estará cerrado, cortocircuitando al condensador $\boldsymbol{C_1}$ del lazo de realimentación del amplificador operacional, $\boldsymbol{A_1}$, haciendo que su salida quede retenida a $\boldsymbol{-V_1}$ ($\boldsymbol{A_1}$ actúa como un seguidor de tensión). Con la subida del pulso de *start/stop* se inicia el ciclo de conversión, se abre el conmutador $\boldsymbol{S_1}$ haciendo que el amplificador operacional, $\boldsymbol{A_1}$, actue como integrador y su salida sea una rampa con pendiente positiva y de valor $\boldsymbol{1/R_1C_1}$.

La salida de este integrador va a dos comparadores, uno que la compara con *tierra* y otro que lo hace con la señal analógica a convertir, $\boldsymbol{V_A}$. Así, cuando la salida del integrador llega a cero, el *comparador 1* cambia el valor de su salida de 0 a 1. Como la salida del *comparador 2* también es 1 ($\boldsymbol{V_A > 0}$ ***volts***), la puerta AND deja pasar los pulsos de reloj al contador binario.

Cuando la rampa supera el valor de la señal analógica de entrada, $\boldsymbol{V_A}$, la salida del *comparador 2* pasa a cero, pasando a valer también cero la salida de la puerta AND y se detiene el contador. La salida del contador en ese momento, $\boldsymbol{n}$, es el valor digital correspondiente el valor de la señal analógica de entrada, $\boldsymbol{V_A}$. Igual que en el caso anterior

$$n = 2^N \frac{v_A}{V_{FS}}$$

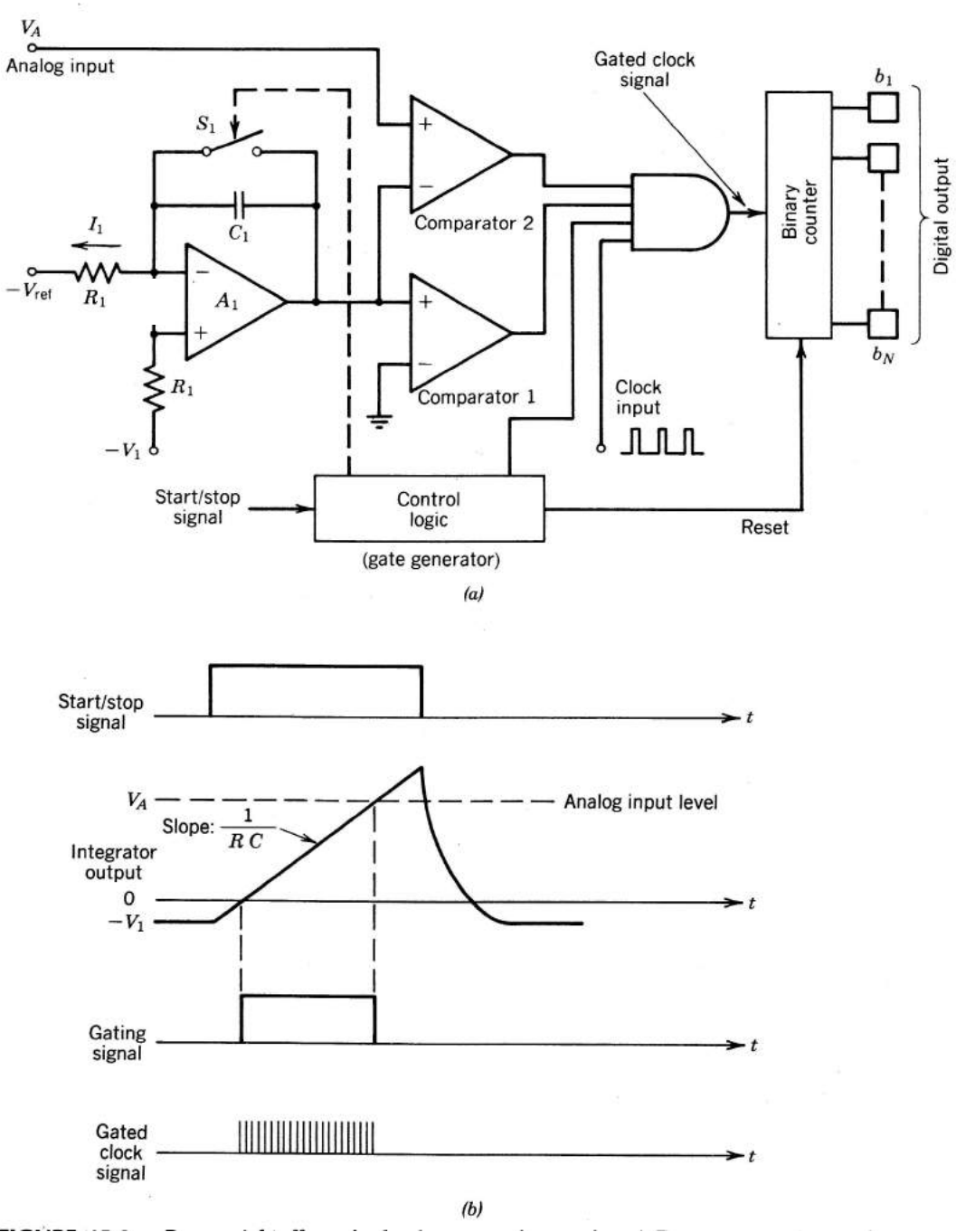


Fig. 11. Diagrama de bloques y formas de las señales en distintos puntos de un conversor A/D de integración en rampa

Como podemos observar, el valor de V_A controla el tiempo que está cargándose el condensador C_1 y por tanto controla el números de pulsos de reloj que deja pasar la puerta AND y que cuenta el contador.

Este tipo de conversor tiene un gran inconveniente y es que aún suponiendo que los comparadores, el integrador y el generador de la tensión de referencia son ideales, la precisión del conversor depende fuertemente del valor absoluto del producto R_1C_1, el cual determina la precisión y estabilidad del factor de escala. Este inconveniente es inherente a todos los conversores del tipo de ***simple rampa***. Este problema se puede evitar usando técnicas de conversión de ***doble rampa.***

Los conversores de ***doble rampa*** son los más usados dentro de los conversores ***A/D de integración***. La figura 12 muestra su diagrama de bloques.

Este circuito opera en dos fases. En la ***fase I*** integra la señal analógica que deseamos convertir, V_A, durante un intervalo de tiempo fijo. En la ***fase II*** integra una tensión fija, V_{ref}, durante todo el tiempo que sea necesario y durante el cual un contador va incrementándose con los pulsos de reloj que le llegan, hasta que el integrador pasa por cero. En ese momento se detiene el contador de forma que su valor será proporcional al valor de la señal analógica de entrada que deseamos convertir a digital. Veámoslo con más de detalle.

Vamos a considerar que la señal analógica a convertir va a variar entre 0 y $-V_{FS}$. Inicialmente el conmutador S_1 está en $-V_A$, mientras que S_2 está cerrado. En estas condiciones en V_X tenemos una tensión ligeramente negativa que podemos considerar prácticamente cero. Con el pulso de inicio (pulso en satrt/stop) comienza la primera fase de conversión es decir, se abre el conmutador S_2 pasando el circuito a funcionar como integrador de la señal analógica de entrada, $-V_A$, durante un tiempo prefijado que suele ser 2^N ciclos de reloj, que lo determina el circuito de control y que es fijo para esta fase de la conversión. Durante este tiempo el integrador genera una rampa de pendiente positiva tal que

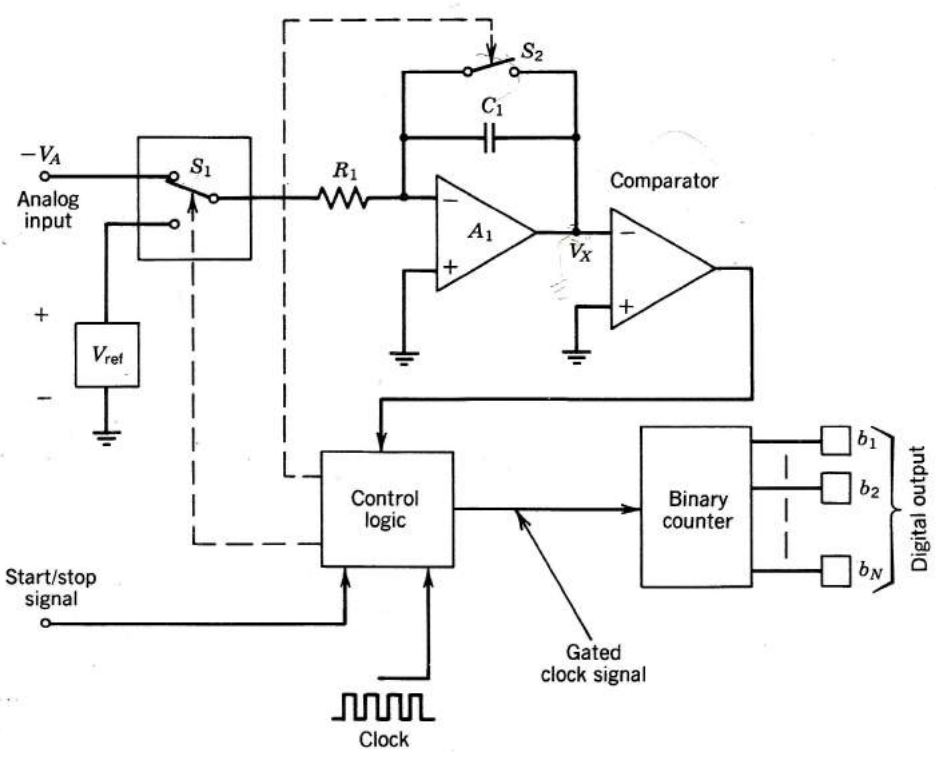
$$\left(\frac{dV_X}{dt}\right)_{fase\ I} = \frac{+V_A}{R_1C_1}$$

Cuando termina esta primera fase, el contador binario, que nos ha de dar la salida en digital y que previamente se ha puesto a cero, empieza a contar a la vez que el conmutador S_1 pasa al terminal de $+V_{ref}$. La salida del integrador, V_X , empezará a decrecer hasta que alcanza el valor de cero, generándose una rampa de pendiente negativa. Así, la pendiente ahora es:

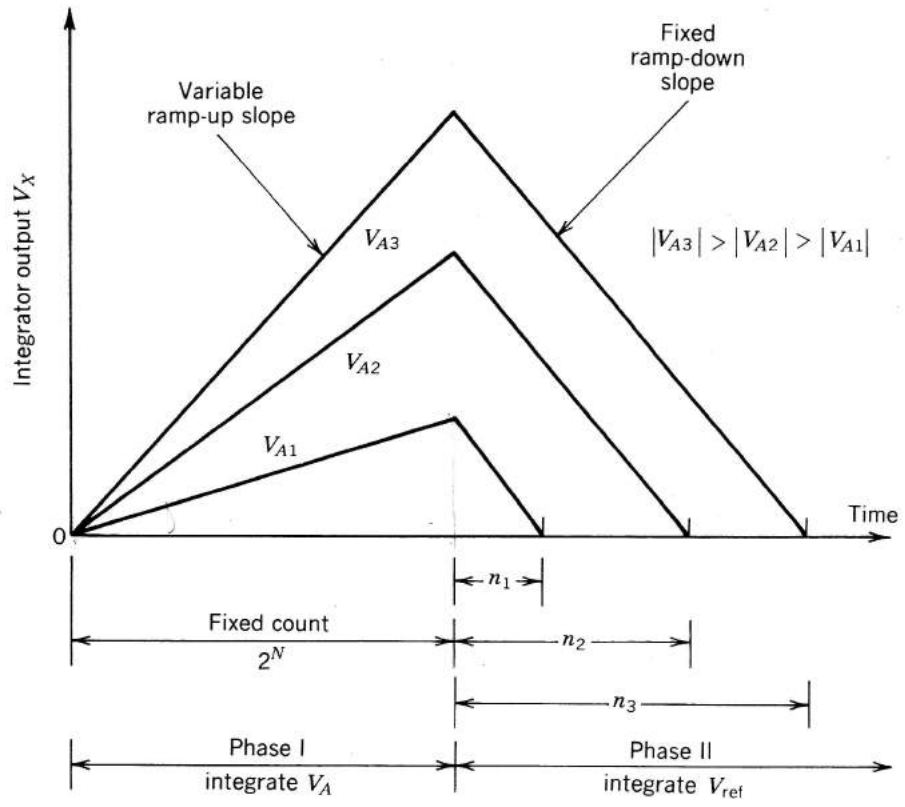
$$\left(\frac{dV_X}{dt}\right)_{fase\ II} = \frac{-V_{ref}}{R_1C_1}$$

Durante esta fase, el contador ha estado contando los pulsos de reloj que le han llegado. La salida del contador es ahora el valor digital equivalente a la señal analógica de entrada.

El comparador genera un pulso negativo y de duración la suma de la duración de las dos fases. Su función es informar al circuito de control de que la conversión ha terminado para que este detenga al contador binario de salida.



(a)



(b)

Fig. 12. (a) Diagrama de bloque de un conversor A/D integrador en doble rampa. (b) Formas de onda a la salida del integrador ($\boldsymbol{V_X}$) para distintos valores de la señal analógica de entrada, $\boldsymbol{V_A}$.

La cantidad ***n*** almacenada en el contador durante la fase de integración de la V_{ref} es el valor digital equivalente de la señal analógica

$$n = -V_A \frac{2^N}{V_{ref}}$$

Obsérvese que el punto clave en el funcionamiento de este tipo de circuitos está en que la rampa de subida tiene una pendiente variable, proporcional al valor de la señal analógica que se quiere convertir, ya que el tiempo que dura la rampa de subida es fijo, mientras que la rampa de bajada tiene una pendiente constante para cualquier valor de V_A y lo que varía en esta segunda fase es el tiempo que tarda en alcanzar el cero puesto que su punto de partida es mayor o menor (figura 12.b) dependiendo del valor de V_A **.**

Este tipo de conversores tiene algunas ventajas para el diseño de conversores de alta resolución:

1. La ***precisión*** de la conversión es independiente del valor de la constante de tiempo del integrador (por ejemplo del producto RC) y de la frecuencia del reloj, ya que estos parámetros afectan por igual a los tiempos de la rampa de subida que a los de bajada.
2. La ***linealidad*** es bastante buena ya que principalmente está determinada por la calidad de la forma de onda del integrador. La no linealidad diferencial es virtualmente eliminada puesto que la función analógica y la forma de onda en rampa permanece continua durante el proceso de conversión. La única contribución a la no linealidad diferencial es la fluctuación del reloj durante el intervalo en el que se está contando.
3. Otra ventaja es el gran ***rechazo al ruido*** procedente de la fuente de alimentación (50 ciclos de la red). Este ruido limita el uso de instrumentación que necesita alta resolución y que se alimenta a partir de la red de potencia, aparece normalmente superpuesto a la señal de entrada y tiene un valor medio nulo. Como durante el proceso de conversión, la señal de entrada es integrada durante un tiempo fijo, podemos hacer este tiempo igual al periodo de la señal de línea (1/50Hz, es decir 20 mseg) o a un múltiplo de este periodo, dando lugar a una gran atenuación de este ruido durante el proceso de integración. Así se puede atenuar este ruido hasta 70 dB.

Debido a las ventajas comentadas previamente, esta técnica de conversión se usa en conversores que son adecuados para aplicaciones que necesitan alta resolución y baja velocidad.

3.3 Conversión Simultanea (paralelo)

Este tipo de conversión es el más rápido y conceptualmente el más simple. Usa un comparador con una tensión de referencia fija para cada nivel de cuantificación en la palabra digital, desde el valor cero hasta el de fondo de escala. Las salidas de estos comparadores entran a un circuito lógico de decodificación que produce la señal digital de salida, como se muestra en la figura 13. Así, para una resolución de ***N*** bits, son necesarios 2^N-1 comparadores separados y por tanto también hay que generar 2^N-1 niveles de referencia. Tiene el problema de que la complejidad del circuito aumenta bastante al incrementar el número de bits del conversor. Un aumento de un bit supone duplicar el número de comparadores. Sin embargo tiene la ventaja de que todos los bits son procesados a la vez por lo que sólo hace falta para la conversión un ciclo de reloj. Debido a

esta propiedad a estos conversores también se les llama ***conversores "flash"*** o ***conversores "flash encoders"***.

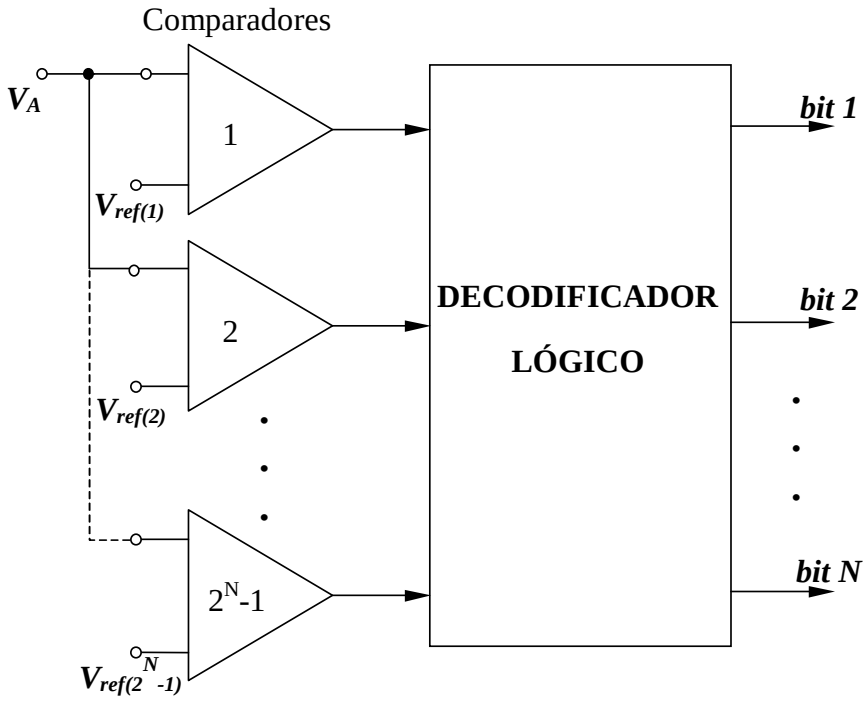


Fig. 13. Diagrama de bloques de un conversor paralelo.

La figura 14 muestra la arquitectura básica de un conversor A/D paralelo de ***N*** bits con más detalle. Los ***2^N-1*** niveles de decisión o tensiones de referencia, que corresponden a los niveles de cuantificación individuales se generan mediante una red de resistencias

Obsérvese cómo, en este método, todos los bits están determinados de antemano. Hay un banco de comparadores diferenciales cada uno de los cuales posee como tensión de referencia una fracción del total. En el ejemplo, la entrada analógica se divide en ocho rangos, de los cuales seis ocupan un intervalo S=Vref/7 y los dos rangos extremos, primero y último, ocupan cada uno un intervalo S/2=Vref/14. En la tabla de la figura 15 se ilustran estos rangos, la salida digital correspondiente y la tensión analógica equivalente a esa salida para ilustrar el error que cometemos en cada intervalo.

Para cada valor de la señal analógica, la salida de los comparadores está en alta hasta un cierto nivel y a partir de ahí está en baja. Estos valores se transfieren a los biestables de un registro de forma síncrona, en las caídas o subidas de los pulsos del reloj. Después hay un decodificador que nos pasa los estados del registro a un código binario de tres bits de acuerdo con la tabla de la figura 15. Así, las salidas digitales son:

$$MSB = Q_4$$

$$2LSB = Q_2 \overline{Q}_4 + Q_6$$

$$LSB = Q_1 \overline{Q}_2 + Q_3 \overline{Q}_4 + Q_5 \overline{Q}_6 + Q_7$$

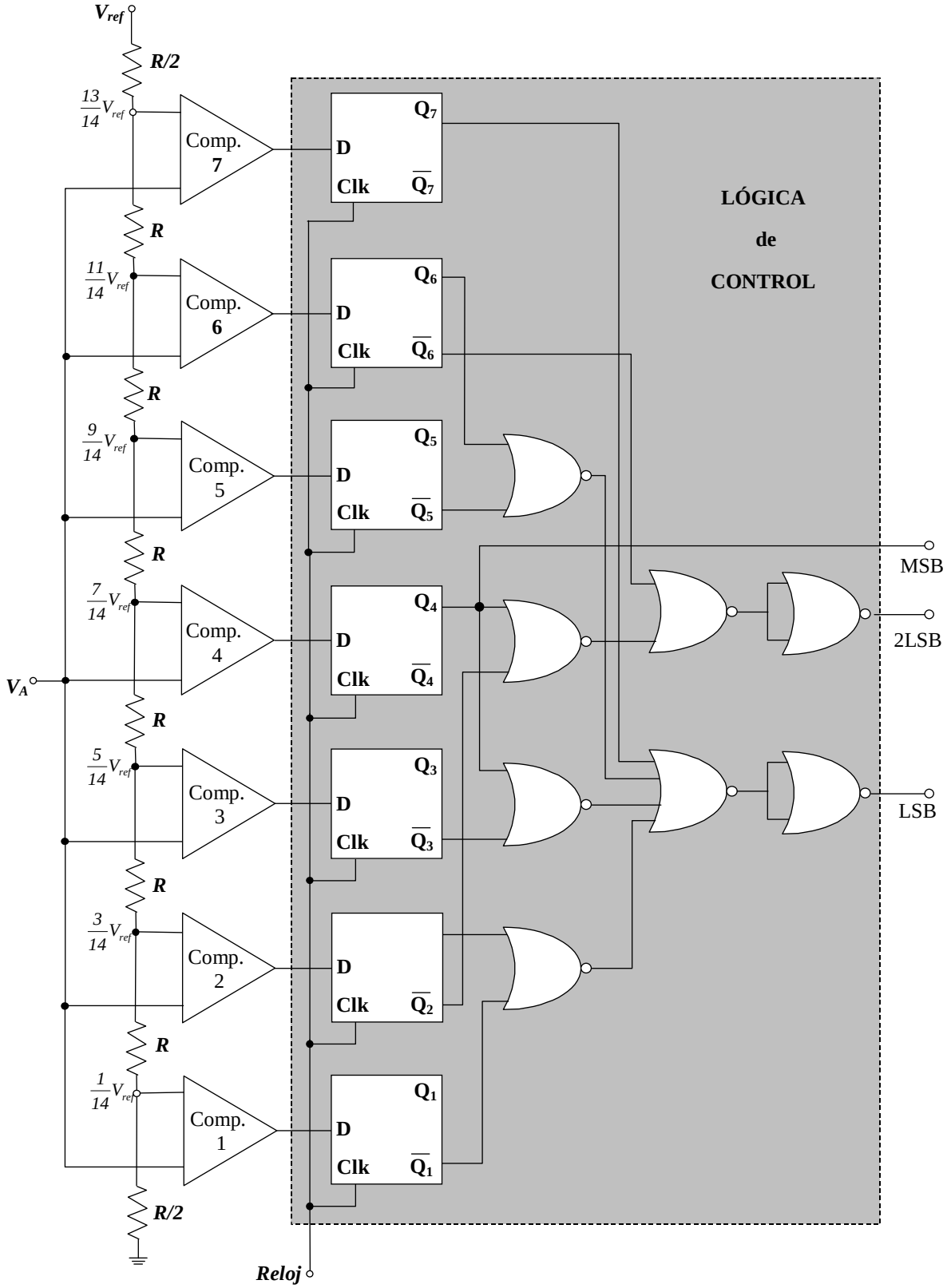


Fig. 14. Circuito completo de un conversor paralelo

Rango de V_A	*Niveles de Referencia*	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	*Salida Digitales* MSB	2LSB	LSB
V_{ref}	S/2	1	1	1	1	1	1	1	1	1	1
$13V_{ref}/14$	S	0	1	1	1	1	1	1	1	1	0
$11V_{ref}/14$	S	0	0	1	1	1	1	1	1	0	1
$9V_{ref}/14$	S	0	0	0	1	1	1	1	1	0	0
$7V_{ref}/14$	S	0	0	0	0	1	1	1	0	1	1
$5V_{ref}/14$	S	0	0	0	0	0	1	1	0	1	0
$3V_{ref}/14$	S	0	0	0	0	0	0	1	0	0	1
$1V_{ref}/14$	S/2	0	0	0	0	0	0	0	0	0	0
0											

Fig. 15. Tabla explicativa del funcionamiento del conversor paralelo de la figura 13

Si la señal analógica de entrada, $V_A(t)$, está entre cero y $V_{ref}/14$ la salida de todos los comparadores está en baja y la palabra digital correspondiente a **000**. Si esta señal digital se convirtiera de nuevo en analógica, obtendríamos un valor cero por lo que el error de cuantificación será como máximo $V_{ref}/14$.

Si la señal, $V_A(t)$, está entre $V_{ref}/14$ y $3V_{ref}/14$, en el rango **S**, la salida digital será **001**. Si pasáramos de nuevo esta palabra al nivel analógico tendríamos:

$$\left(1 \cdot 2^0 + 0 \cdot 2^1 + 0 \cdot 2^2\right)\frac{V_{ref}}{7} = \frac{V_{ref}}{7}$$

Es decir, es este intervalo, el error de cuantificación no será mayor de $S/2=V_{ref}/14$.

Este tipo de conversor, puede operar también en modo asíncrono, sin el registro de salida, de forma que el código de salida varia de acuerdo con el valor en ese instante de la señal analógica de entrada.

4. Tipos de Conversores en Lazo Cerrado

En los métodos que hemos estudiado en el apartado anterior no existía ningún mecanismo en el circuito que nos permitiera saber como había terminado el proceso de conversión para cada valor de la señal analógica. Eran métodos de conversión en lazo abierto.

Ahora vamos a estudiar otros métodos que usan la realimentación para medir y minimizar el error del proceso de conversión. Como entra una señal analógica y sale digital, la comparación necesaria para calcular el error nos obliga a obtener un nuevo valor analógico a partir de la palabra digital para comparar dos señales analógicas. Por eso es usual incluir un conversor D/A en el lazo de control de los conversores A/D que usan "algoritmos" en lazo cerrado.

El diagrama de la figura 16 ilustra la estructura general de estos métodos de conversión. El lazo se cierra al comparar la señal analógica de entrada, $V_A(t)$, con otra generada internamente, $V_d(t)$. El resultado de la comparación se lleva a la lógica de control

que determina si el proceso de comparación debe seguir o parar, sacando en este caso el resultado. Estos conversores A/D incluyen un conversor D/A tipo red (***R- 2R***) y suelen ser síncronos.

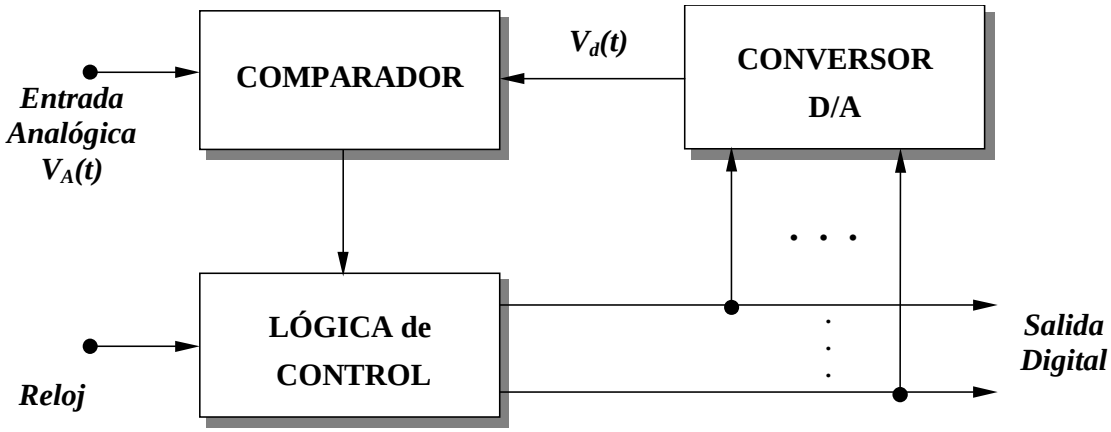


Fig. 16. Esquema de conceptual de los conversores A/D en lazo cerrado.

Estudiaremos dos tipos básicos:

- ***Rampa-contador***
- ***Aproximaciones sucesivas***

4.1. Rampa-contador

El esquema conceptual de estos conversores se muestra en la figura 17. El ciclo de conversión comienza con la carga del contador de N bits desde cero hacia 2^N, a partir de los pulsos del reloj. La salida del contador va a un conversor D/A que genera una rampa escalonada que entra a un comparador junto con la señal analógica externa, V_A. Mientras la señal del contador es inferior, la salida del comparador esta en alta, por ejemplo. En cambio, cuando es mayor o igual que la externa, el comparador conmuta y pasa a baja su salida, cerrando la entrada de nuevos pulsos al contador y facilitando la salida de su último estado. Este último estado que ha parado el proceso de incrementar el contenido del contador es el valor "digital", V_o, igual al analógico de entrada, V_A.

Este tipo de conversor tiene una limitación en el período del reloj, T_C, que debe satisfacer la siguiente relación:

$$T_C > \Delta T + t_{DA} + t_{CD}$$

donde ΔT es el valor del retardo de propagación en el contador en el peor de los casos, t_{DA} el retardo en el conversor D/A y t_{CD} el retardo en el comparador. Si el periodo del reloj es superior a este valor mínimo, la salida del comparador tendrá tiempo de llegar al circuito lógico que controla el paso de pulsos al contador antes de que llegue un nuevo pulso de reloj.

Una característica distintiva de este método es que al iniciar un nuevo ciclo de conversión, no se parte de cero sino del último valor convertido. Como el contador binario es reversible, si el nuevo valor analógico es inferior al anterior se decrementa el contenido del contador. Si es superior, se incrementa, dependiendo del signo de la señal de salida del conparador (del "error").

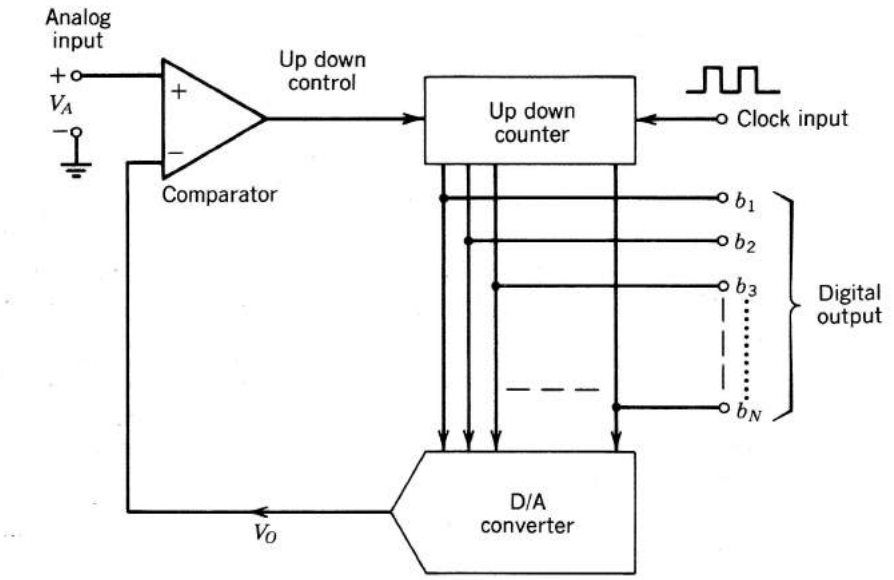


Fig.17. Esquema conceptual de los conversores en lazo cerrado tipo rampa-contador. Obsérvese que la rampa es digital, es la señal en escalera creciente que genera el D/A ante las sucesivas configuraciones crecientes del contador binario.

Para que la salida pueda recorrer el fondo de escala, pasando de ***0*** a 2^N, se consume un tiempo razonable ya que hay que esperar los 2^N-1 ciclos de reloj necesarios para cargar el contador. Sin embargo, para señales variables en torno a un cierto punto de funcionamiento estático, el tiempo necesario para la conversión es muy bajo, ya que basta con esperar los pocos pulsos de reloj necesarios para convertir el incremento o decremento correspondiente a la pequeña señal que se superpone al punto de funcionamiento estático. Esta característica hace que a estos conversores se les llame de ***"seguimiento"*** o ***tipo servomecanismo***.

Este procedimiento de conversión A/D es bueno cuando se necesita mucha precisión, ya que aumentar el número de bits no conlleva un aumento en la complejidad del circuito. Lo único que aumenta es el tiempo necesario para realizar una conversión (2^N periodos de reloj para ***N*** bits). Así, al aumentar en un bit el poder de resolución del conversor, duplicamos el tiempo de conversión. Esta situación de compromiso entre ***velocidad*** y ***precisión*** suele ser común a todos los algoritmos de conversión.

La causa de la baja velocidad de las primeras versiones de estos conversores, que usaban contadores unidireccionales estaba en que al finalizar una conversión, el contador pasaba a cero y se iniciaba de nuevo la cuenta hacia 2^N, independientemente del valor de la última muestra. Para aumentar la velocidad se usan ***contadores bidireccionales*** de forma que al finalizar un proceso de conversión el contador no pasa a cero sino que incrementa o decrementa su contenido en función del valor de la muestra siguiente tal como hemos comentado previamente.

El uso de contadores bidireccionales es particularmente adecuado cuando se está convirtiendo un solo canal, ya que no es de esperar saltos bruscos en una señal. Sin embargo, si el proceso de conversión actúa sobre la salida de un multiplexo, su eficacia y velocidad es mucho menor ya que las muestras sucesivas proceden de fuentes de señal independientes y por consiguiente es de esperar cualquier salto entre los valores de dos muestras sucesivas.

4.2. Aproximaciones Sucesivas

Este método de conversión es muy usado por el equilibrio que alcanza entre ***precisión*** y ***velocidad***, que lo hace idóneo para un amplio rango de aplicaciones. Proporciona valores muy altos del producto precisión por velocidad y es muy adecuado para soluciones integradas en tecnología MOS. De hecho, hay circuitos de este tipo, como el ADC800, que llevan en el mercado más de 20 años.

El conversor A/D por aproximaciones sucesivas opera de acuerdo con el esquema conceptual de la figura 16, del comienzo del apartado 4, como un lazo de control que va comparando una señal analógica con un código digital, sólo que ahora el código digital no se genera de forma lineal, cargando un contador a partir de un tren de impulsos, sino dividiendo el rango dinámico de fondo de escala bit a bit . La señal está "por encima" o "por debajo" de la mitad del fondo de escala. Si está por encima, está en la mitad superior o en la inferior etc… Así, en vez de necesitar $\boldsymbol{2^N}$ ciclos de reloj, sólo necesitamos $\boldsymbol{N}$ ciclos y para incrementar la precisión en un bit, no incrementaremos el tiempo de conversión hasta el doble ($\frac{2^{N+1}}{2^N} = 2$) sino en 1, (***N+1-N=1***). Esta es la clave del método. El resto es análogo al método anterior. En el proceso de conversión A/D bit a bit también se usa un conversor D/A en el lazo de realimentación, un comparador y una lógica de control interno para decidir el valor de cada bit en $\boldsymbol{N}$ pasos. Veamos ahora de forma más detallada el funcionamiento de estos conversores para el caso de 3 bits.

En la figura 18 se muestra el árbol de decisión binario que se recorre para llegar a cada una de las configuraciones finales (**111**, …, **001**, **000**). La trayectoria marcada con una línea de puntos corresponde a las decisiones que nos llevan a la configuración **101**.

Para comprender mejor el funcionamiento es conveniente que el alumno considere a la vez la figura 19 y 20 donde aparecen, respectivamente, el circuito completo y el cronograma de este conversor.

Inicialmente, se genera internamente la palabra **100**, con el bit más significativo en alta. Este valor pasa por el D/A, generándose la $\boldsymbol{V_d}$ correspondiente a esta palabra y se compara con la señal externa, $\boldsymbol{V_A(t)}$. Si $\boldsymbol{V_A(t)}$ es mayor que **100**, se deja el bit más significativo en alta y en el siguiente paso se comienza poniendo en alta el segundo bit y repitiendo la comparación. En cambio, si $\boldsymbol{V_A(t)}$ es menor que la $\boldsymbol{V_d}$ correspondiente a **100**, se pasa a baja este bit y se repite la comparación con **010**. Este proceso de puesta a alta, comparación y borrado o puesta a cero del siguiente bit se repite $\boldsymbol{n}$ veces (tres en el ejemplo).

El conversor utiliza cinco intervalos de reloj para realizar una conversión. Tres de estos intervalos se usan para determinar el valor de los tres bits, durante el cuarto se lee la salida digital y, finalmente, en el quinto se pone a cero el conversor y se le deja preparado para realizar la siguiente conversión. Como siempre, durante la conversión la entrada permanece constante y cuando se está leyendo el resultado de la conversión de una muestra, se toma la siguiente. Es decir, la salida $\boldsymbol{Q_E}$ debe controlar los conmutadores del circuito de muestreo-retención.

Los biestables FFA a FFE están conectados de forma que constituyen un contador en anillo en el que solo un biestable está en alta en cada momento. Este estado de alta se desplaza de FFA a FFE. Por otro lado, los biestables FF1 (LSB), FF2 (2SB) y FF3 (MSB)

almacenan las configuraciones de prueba que van al D/A y al exterior al final de la conversión.

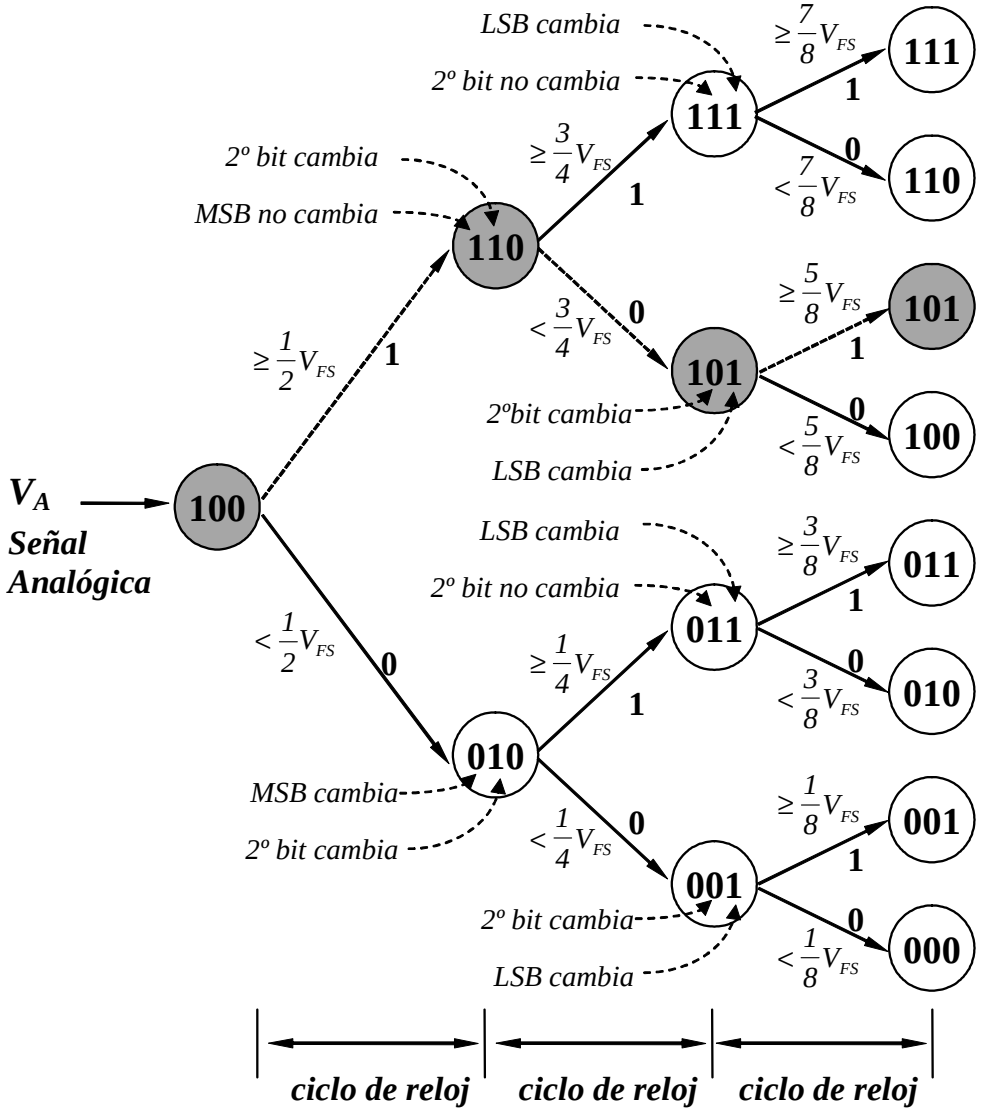


Fig. 18. Arbol binario de conversor A/D de aproximaciones sucesivas. Obsérvese que bastan 3(***N***) ciclos de reloj para alcanzar el valor digital correspondiente al analógico con el que se compara para una precisión de 3(***N***) bits.

El ciclo de conversión comienza con:

1) $Q_A=1;\ Q_B= Q_C =.\ Q_D= Q_E=0$ Entonces, FF3 pasa a alta ($Q_3=1$) y FF2 y FF1 a baja ($Q_2= Q_1=0$). Así, a la entrada del conversor D/A tenemos **100** y a la salida, $V_d= 4V_{ref}$. Este es el valor que se compara con $V_A\ (t)$, de forma que:

   $V_A\ (t) \geq V_d \Rightarrow C_0= 0$

   $V_A\ (t) < V_d \Rightarrow C_0 = 1$

2) En el siguiente ciclo de reloj, $Q_B=1;\ Q_A= Q_C =.\ Q_D= Q_E=0$, de forma que por una parte FF2 pasa a alta y FF3 permanece en alta si $V_A\ (t) > VD$ ($C_0 =0$) o pasa a baja si $C_0 = 1$. En el primer caso a la entrada del D/A tenemos la palabra **110** y en el segundo, **010**. Sea cual fuese el valor se repite ahora la comparación con $V_A(t)$

generándose un nuevo valor de C_0, en principio distinto y pasando a calcular el valor del tercer bit.

3) En el tercer ciclo de reloj, $Q_C=1$ de forma que pasa a alta FF1 y se facilita la puerta G2 para que deje en alta o pase a baja al biestable FF2 dependiendo del resultado de la última comparación.

4) El cuarto ciclo es análogo a los anteriores.

5) Ahora $Q_E=1$ con lo que se facilitan las puertas G4, G5 y G6 y se saca la palabra digital resultado del proceso de conversión.

Al siguiente pulso de reloj se inicia un nuevo ciclo de conversión, $Q_A=1$, a la vez que se ponen a cero FF2 y FF1. Para N bits hemos necesitado ($N+2$) períodos de reloj, frente a los 2^N que necesitaba el método de rampa-contador.

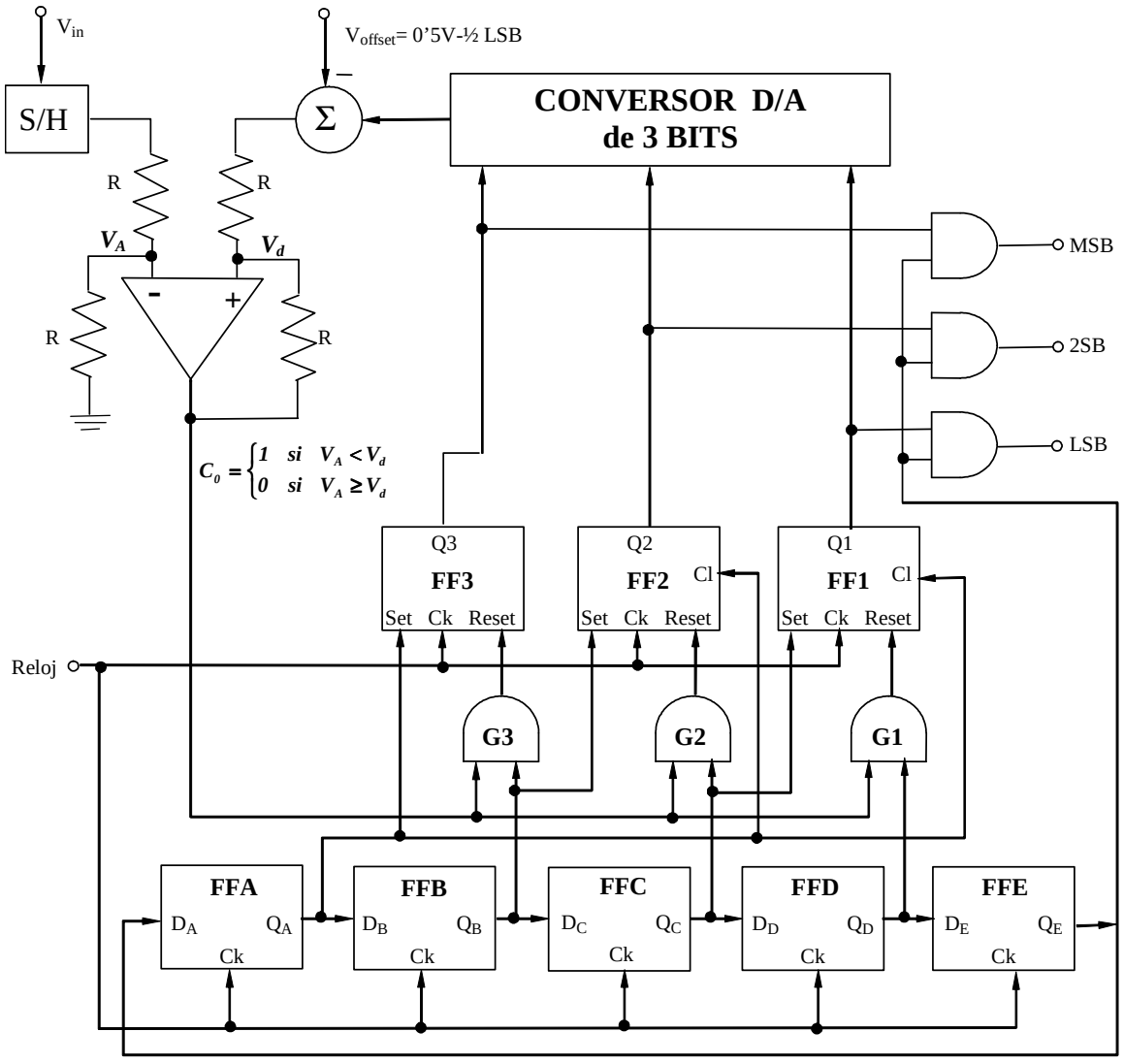


Fig. 19. Circuito de un conversor A/D de aproximaciones sucesivas.

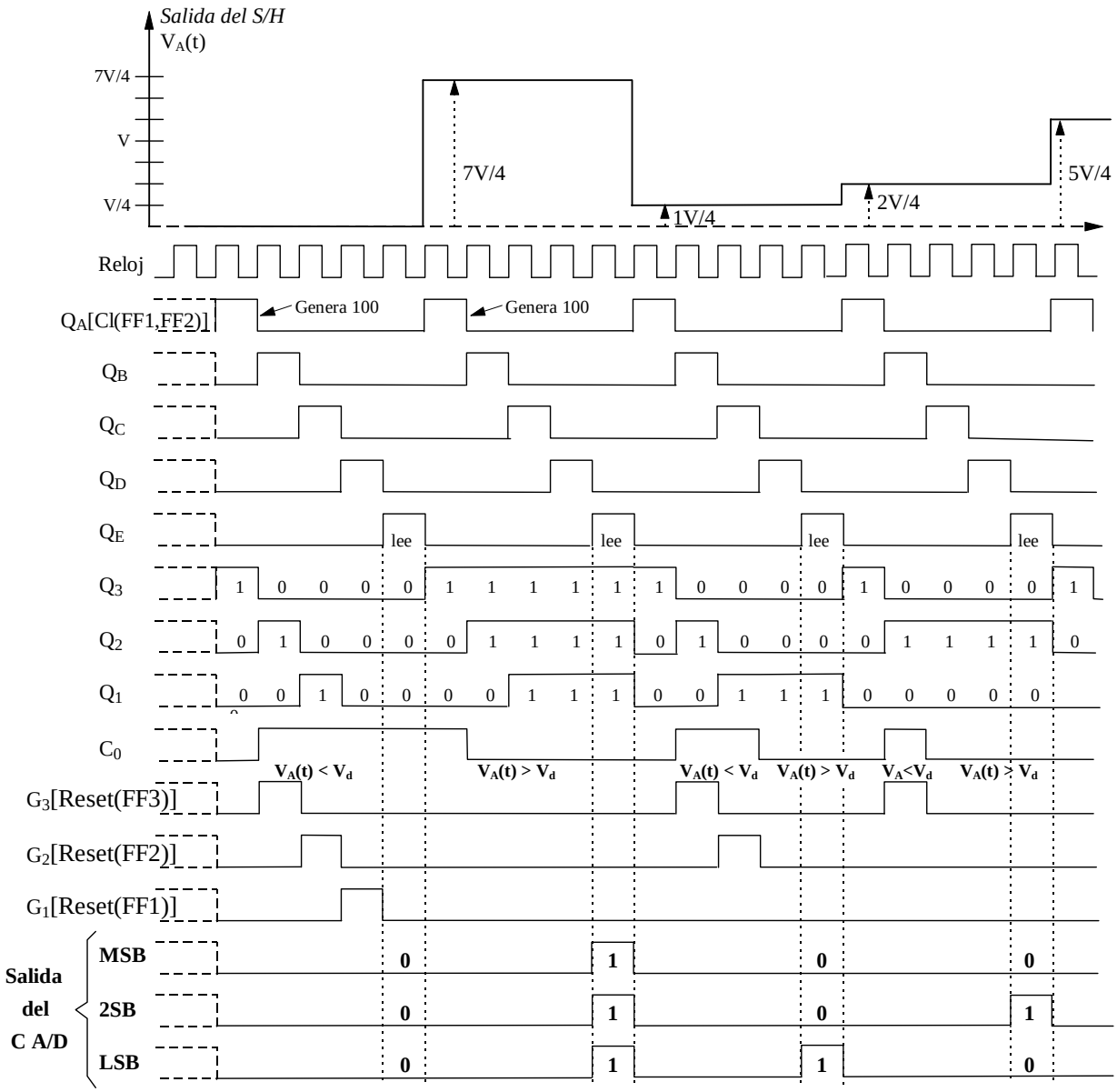


Fig. 20. Cronograma del circuito de la figura 19. Obsérvese con detenimiento la evolución temporal de las señales en los distintos puntos de interés del circuito. En particular, el funcionamiento de la lógica de control que decide de forma sucesiva el valor de MSB, del bit intermedio, 2LSB, y del LSB.

Este método de conversión se puede simplificar usando registros de aproximaciones sucesivas (SAR) que incluyen toda la lógica de control de forma que sólo necesitamos añadir el conversor D/A y el comparador. La figura 21 muestra un ejemplo para 10 bits (Analog Devices AD-571)

Este circuito integrado ya contenía, a comienzos de los 80, todos los bloques funcionales esenciales para la síntesis de un conversor de aproximaciones sucesivas. El conversor D/A, el comparador y las tensiones de referencia y toda la parte digital.

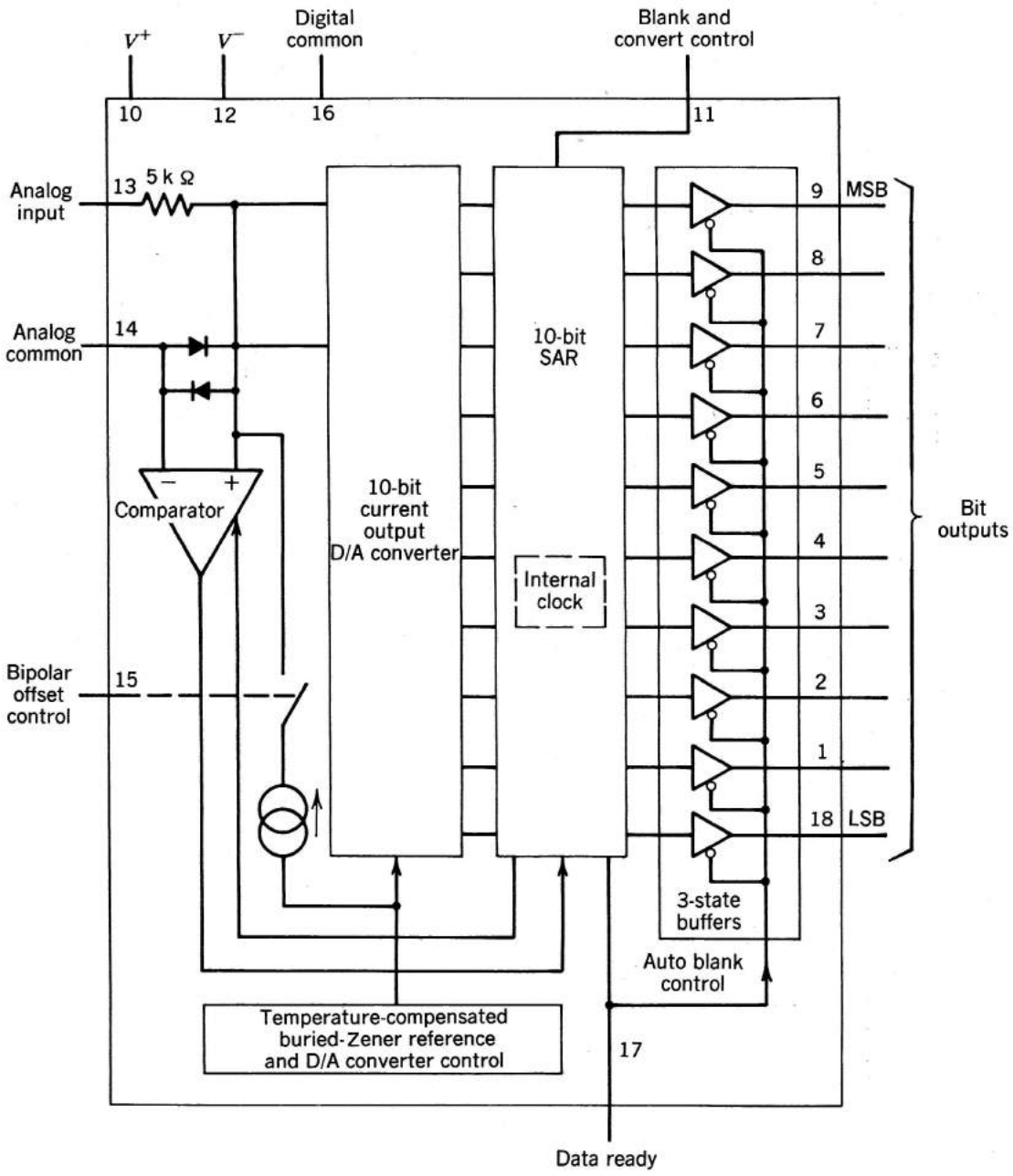


Fig. 21. Diagrama de bloques del circuito AD-571, conversor de aproximaciones sucesivas de 10 bits que incluye un registro SAR.

5. 5. Criterios de Selección de un Conversor A/D y Ejemplos

En los apartados previos de este capítulo hemos visto la posición de los conversores A/D en el esquema general de un sistema de tratamiento digital de señales analógicas, las características que definen un conversor A/D ideal y las fuentes de error que apartan a los conversores reales de los ideales. Después hemos estudiado distintos métodos de conversión usando como criterio de clasificación el carácter de "***lazo abierto***" o "***lazo cerrado***" de la configuración. También hemos repetido en varios puntos la situación de compromiso que siempre hay que resolver entre "***precisión***" y "***velocidad***". Evidentemente, la solución ideal sería optimizar a la vez precisión y velocidad de conversión. Esto complica enormemente el diseño por lo que hay tres alternativas básicas:

1. Alta precisión y baja velocidad.
2. Alta velocidad y valores más modestos en la precisión.
3. Soluciones intermedias, para aplicaciones de propósito general (tipo aproximaciones sucesivas) que optimizan el producto velocidad por precisión con valores altos de ambos parámetros.

Cuando el alumno ha llegado a este punto, damos por supuesto que conoce los principios básicos y las soluciones académicas al problema de la conversión. La siguiente etapa, como siempre, es pasar del análisis al diseño y tomar contacto con las soluciones integradas que ofrecen las distintas casas comerciales en sus catálogos, en general accesibles también a través de la red. Es difícil y probablemente innecesario plantear aquí un panorama completo de los circuitos A/D. Creemos que es suficiente con ilustrar algunos criterios representativos que sirvan como "pista" para, mutantis mutandis, repetir el proceso cuando en el posterior ejercicio profesional sea necesario pasar de una descripción de las especificaciones funcionales que caracterizan un diseño a la selección de los circuitos más adecuados para llevarlo a cabo.

El proceso de selección se puede estructurar a partir de una lista de factores ordenada por su importancia relativa[3]:

Factores Primarios.

1. Nivel de ***precisión*** necesario.
2. ***Resolución*** (nº de bits) necesaria.
3. ***Características de la señal analógica*** de entrada (espectro, pequeña señal, salida de un multiplexo con potenciales saltos bruscos, ...).
4. ***Velocidad*** de conversión necesaria.
5. ***Condiciones ambientales*** donde deberá ser robusto y fiable el conversor.
6. Necesidad (o no) de un ***A/D de seguimiento*** (track & hold).

Factores Secundarios.

7. Necesidad de ***referencia*** externa o interna.
8. Requerimiento de la ***interfaz digital***.
9. ***Forma deseada para la salida*** digital
10. ***Condiciones de temporización*** (cronograma del proceso de conversión hasta conseguir un dato válido a la salida, lógica síncrona, etc...).

Para evaluar la ***precisión*** necesaria en un A/D hay que considerar primero la precisión necesaria en todo el sistema. Por ejemplo, si la precisión global debe ser del 0'012% (12

[3] L. Gaddy. "Selecting an AD Converter". Burr-Brown. Application Bulletin (AB-098), 1995.

bits), el conversor A/D necesitará un valor mayor, por ejemplo 0'006% (13 bits). Además no debemos confundir resolución con precisión. La resolución sólo hace referencia al número de "estados" o configuraciones de escalonamiento en el que queremos ajustar los distintos valores de la señal analógica. Si este número es 2^N, decimos que el conversor A/D tiene N bits de resolución. En cambio, la precisión indica hasta que punto el conversor real se aproxima a estos límites ideales. Ya comentamos al comienzo del tema que la precisión se mide en el dominio del tiempo en términos de un conjunto de ***errores estáticos*** (error de offset, error de ganancia y errores de no linealidad differencial e integral). La figura 22, resume estos cuatro errores y hace evidente la diferencia entre el número de "escalones" de la escalera, (2^N), (resolución), y la forma en la que la característica de transferencia real se aleja de la ideal (precisión).

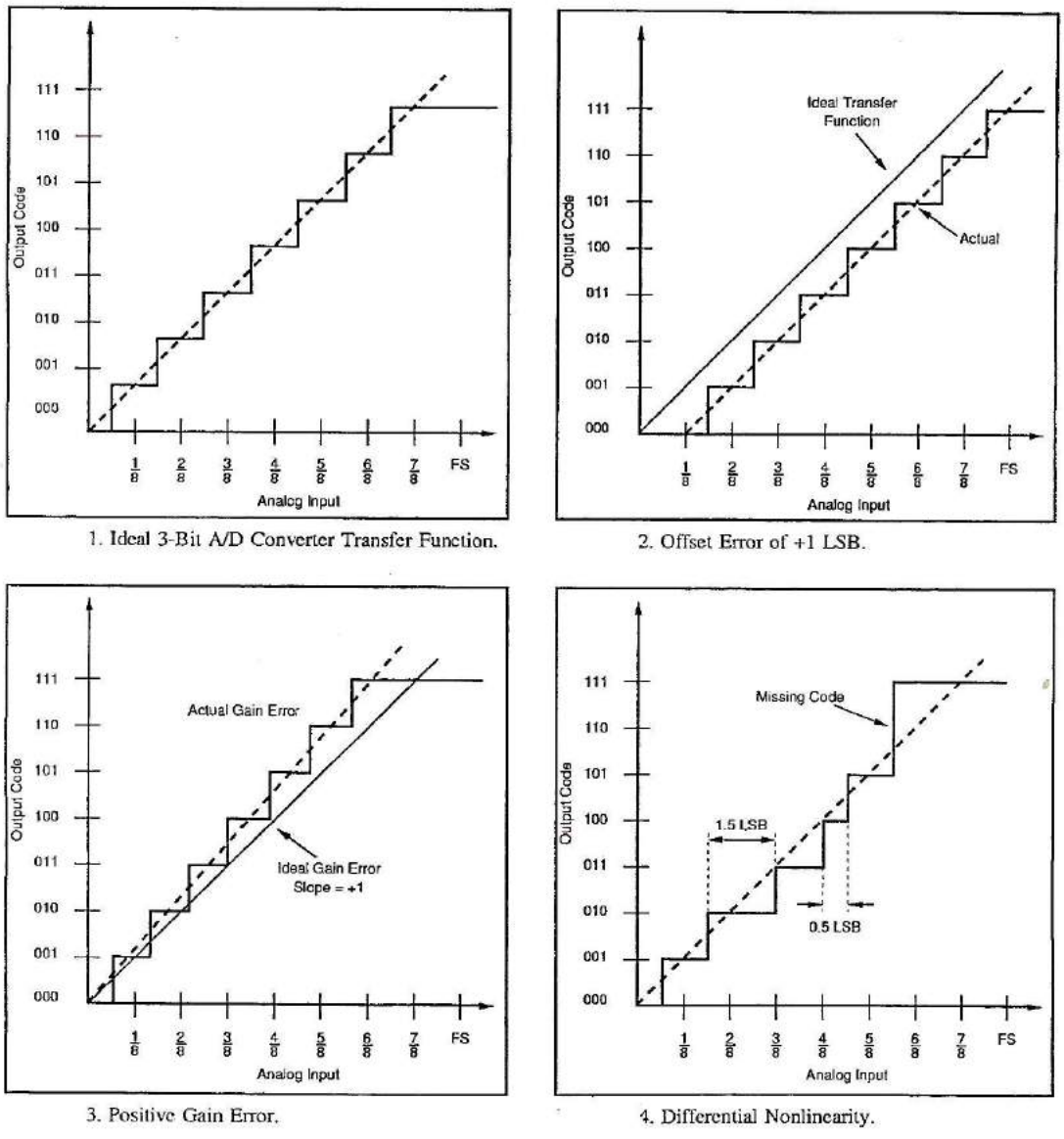


Fig. 22. Resumen de los cuatro tipos de error estático en la conversión A/D. Volver al comienzo del tema para ver una descripción del significado de cada uno de ellos.

La ***velocidad de conversión*** se caracteriza en términos del valor máximo de la frecuencia de muestreo a la que puede trabajar un determinado conversor. Todo el proceso

de conversión de la salida del retenedor tras una muestra debe acabar antes que llegue la muestra siguiente. Así, si un determinado conversor acepta un reloj de conversión de hasta 100 KHz, decimos que toma $100 \cdot 10^3 = 10^5$ muestras por segundo. O lo que es equivalente, que su tiempo de conversión es de 10 μseg. De aquí se deduce también los límites dinámicos de la señal analógica a convertir (recordar el teorema de Shannon, el "aliasing", etc...).

Las otras características de la señal analógica tienen que ver con su ***rango dinámico***, las "excursiones" previstas, si procede de un solo canal (con lo que no hay que esperar saltos bruscos) o de varios (con lo que al multiplexar pueden presentarse secuencias de valores vecinos muy distintos ya que proceden de señales diferentes), etc... Si la señal tiene discontinuidades, la elección debe centrarse en conversores A/D de conversión "en un paso", o en muy pocos pasos tipo "registro de aproximaciones sucesivas" (SAR) o mejor, tipo paralelo, ya que los A/D tipo rampa-integrador o doble rampa tienden a integrar las discontinuidades de la señal, dando lugar a salidas erróneas.

Veamos ahora algunos ejemplos. Por razones pedagógicas, mostramos primero el ADC1210 de aproximaciones sucesivas en tecnología CMOS y con gran versatilidad en el rango dinámico y en las configuraciones de la señal analógica de entrada y en los formatos digitales de la salida.

Después presentamos los datos de la versión actual de la serie 800 de National, El ADC08161, con técnica de conversión en varios pasos y del ADS7818 de Burr-Brown. Finalmente, mostramos los datos del ADS800, también de Burr-Brown pero trabajando a 40 MHZ.

Lo importante no son estos ejemplos sino ilustraros la forma que tienen los datos de catálogo que, como recordareis de temas anteriores, podéis encontrar en las direcciones:

Analog Devices:	http://www.analog.com
National Semiconductor:	http://www.national.com
EXAR:	http://www.exar.com
Texas Instrument:	http://www.ti.com
Burr-Brown:	http://www.burr-brown.com

La mayoría de las casas comerciales ofrecen una estructura en árbol como el de la figura 23 en el que primero clasifican los circuitos y después los ordena de acuerdo con una lista de criterios análogos a los expuestos al comienzo de este apartado.

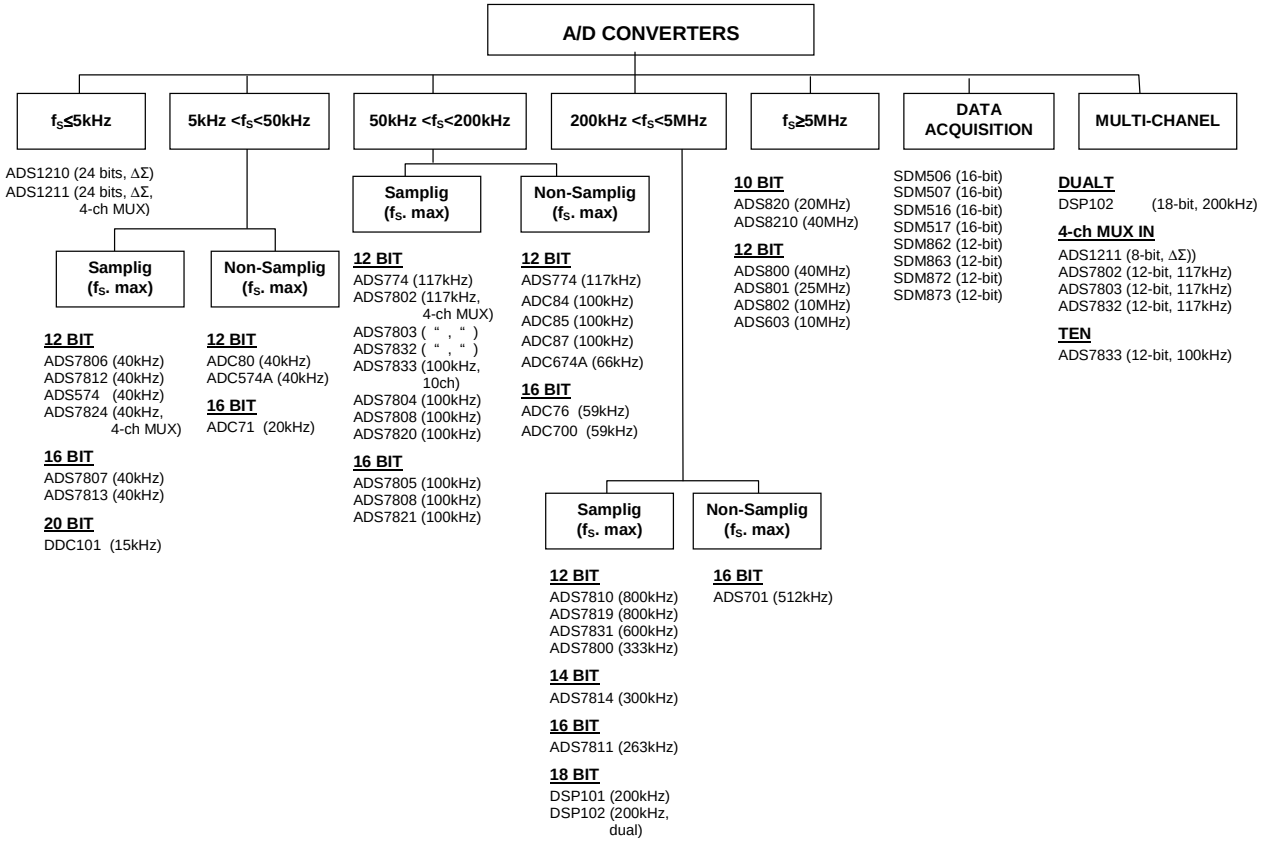


Fig. 23. Ejemplo de clasificación de distintos tipos de conversores A/D.

Application of the ADC1210 CMOS A/D Converter

National Semiconductor
Application Note 245
April 1986

INTRODUCTION

The ADC1210 is the answer to a need for analog to digital conversion in applications requiring low power, medium speed, or medium to high accuracy for low cost. The versatile input configurations allow many different input scale ranges and output logic formats.

The wide supply voltage range of 5V to 15V readily adapts the device to many applications. The very low power dissipation yields remarkable conversion linearity over the full operating temperature range. Table I below summarizes the typical performance of the ADC1210.

TABLE I. ADC1210 Performance Characteristics

Resolution	12 bits
Linearity Error, $T_A = 25°C$	±0.018ç% FS MAX
Over Temperature	±0.0ç66 % FS MAX
Full Scale Error, $T_A = 25°C$	0.2% FS MAX
Zero Scale Error, $T_A = 25°C$	0.2% FS MAX
Quantization Error	±½ LSB MAX
Conversion Time	200 μs MAX

This note expands the scope of application configurations and techniques beyond those shown in the data sheet. The first section discusses the theory of operation. The remaining sections are devoted to applications that extract the optimum potential from the ADC1210.

THEORY OF OPERATION

Like most successive approximation A to D's, the ADC1210 consists of a successive approximation register (SAR), a D to A converter, and a comparator to test the SAR's output against the unknown analog input. In the case of the ADC1210, these elements are connected to allow unusual versatility in matching performance to the user's applications.

The SAR is a specialized shift register programmed such that a start pulse applies a logical low to the most significant bit (MSB) and logical highs to all other bits, thus applying a half scale digital signal to the DAC. If the comparator finds that the unknown analog input is below half scale, the low is shifted to the second bit to test for quarter scale. If, on the other hand, the comparator finds that the analog input is above half scale, the ''low'' state is not only shifted to the second bit, but also retained in the MSB, thus forming the digital code for three quarters scale. Upon completing the quarter (or three-quarter) sacle test, the next clock pulse sets the SAR to test either ⅛, ⅜, ⅝, or ⅞ full scale, depending on the input and the previous decisions. This successive half-the-previous-scale approximation sequence continues for the remaining lower order bits. The thirteenth clock pulse shifts the test bit off the end of the working register and into the conversion complete output. *Figure 1* shows the schematic diagram of the device.

OPERATING CONFIGURATIONS

Figures 2 through *5* show four operating configurations in addition to those presented in the data sheet.

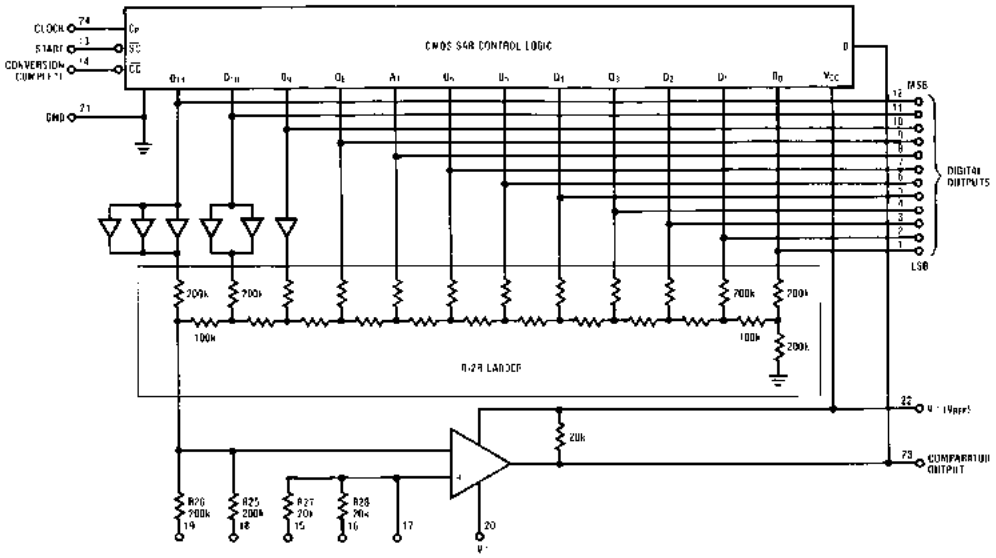


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FIGURE 1. Schematic Drawing

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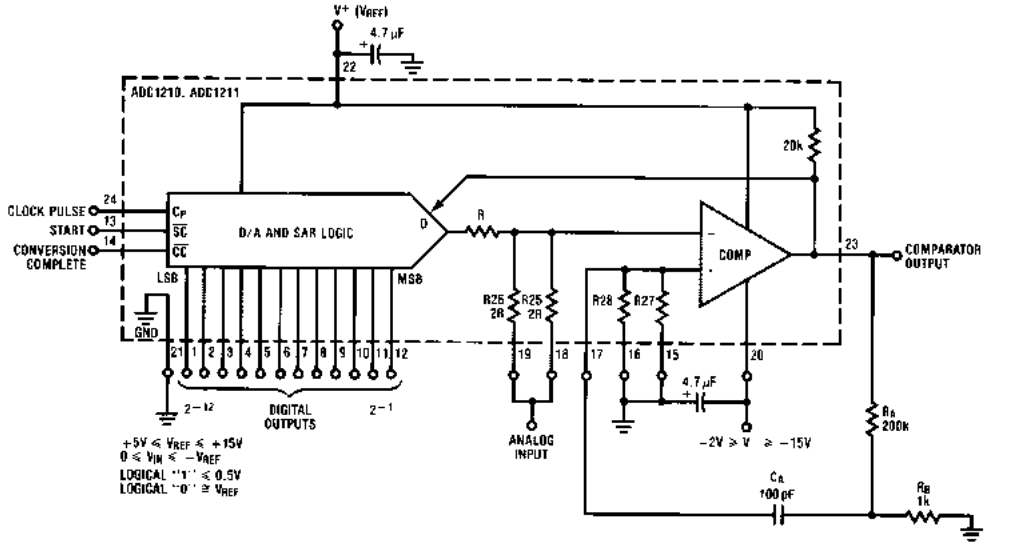

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FIGURE 2. Complementary Logic, 0V to $-V_{REF}$ Input

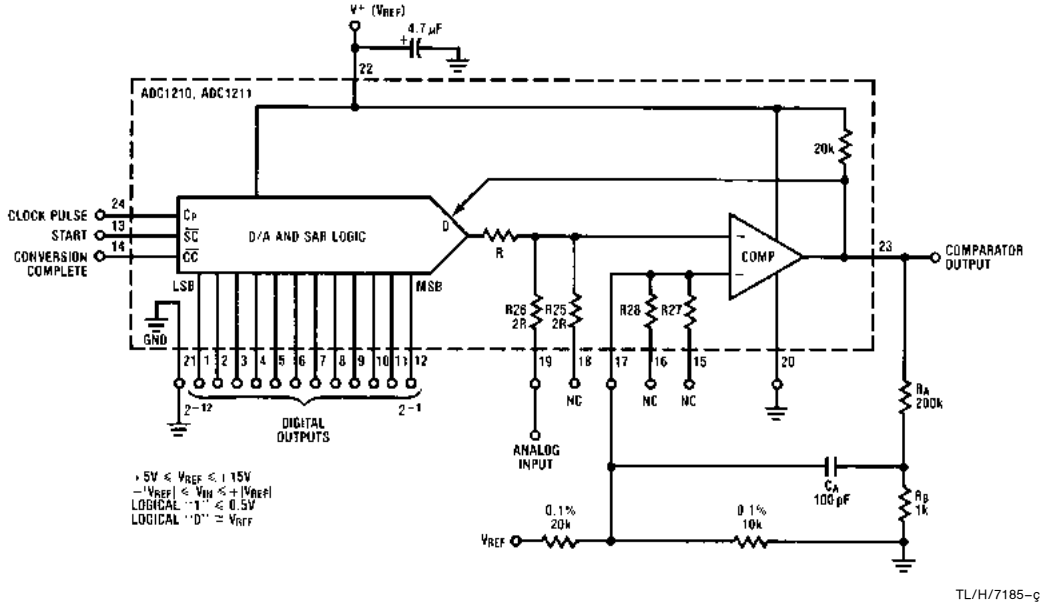

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FIGURE 3. Complementary Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

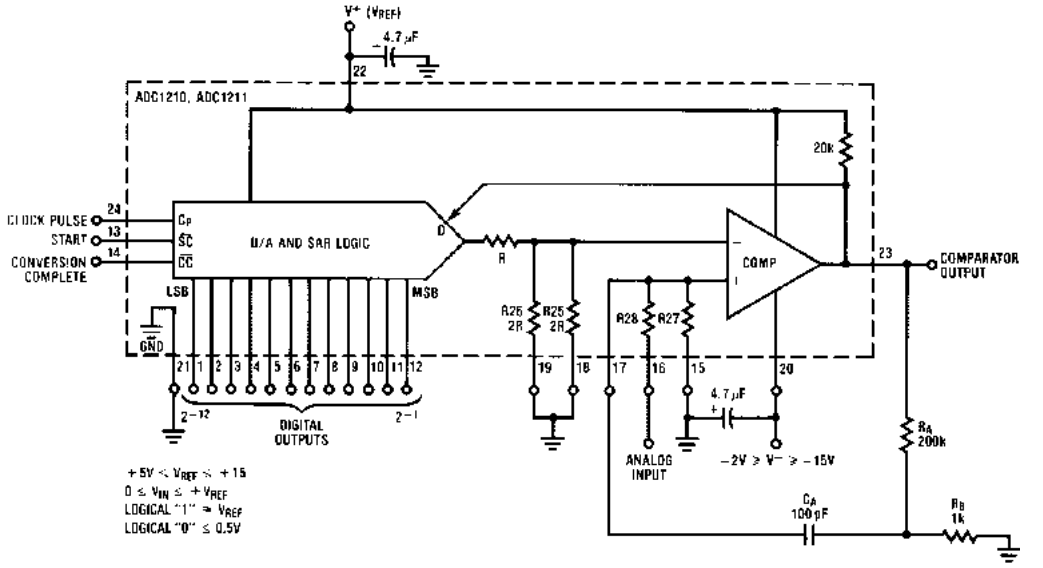

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FIGURE 4. Positive True Logic, 0V to $+V_{REF}$ Input

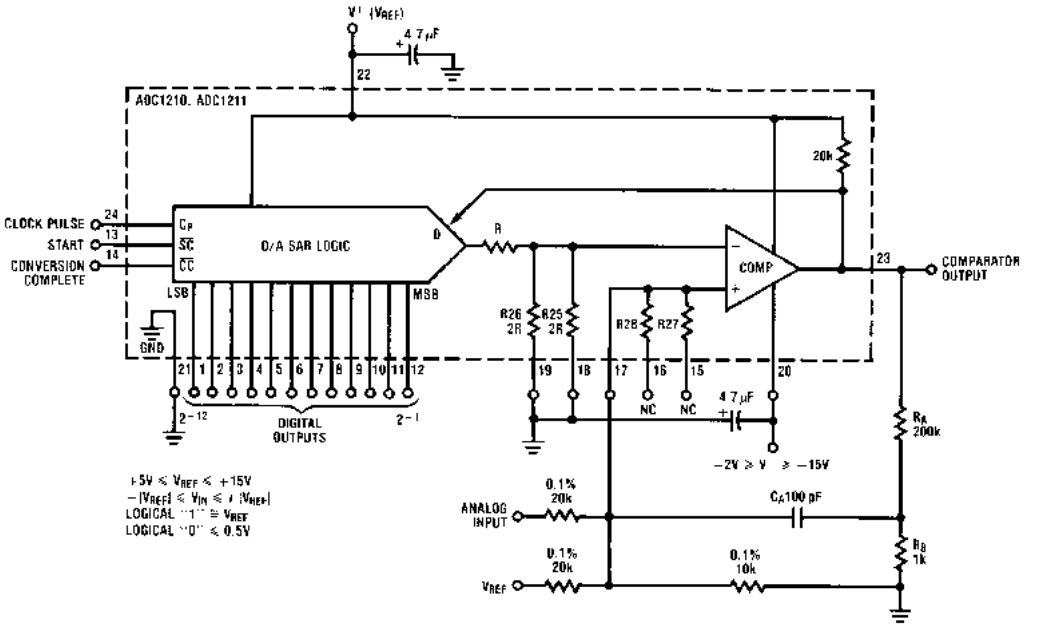

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FIGURE 5. Positive True Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

DESIGN CONSIDERATIONS

To Complement, or Not to Complement

Of the two recommended logic configurations, the complementary version is preferred. It provides greater accuracy than the straight binary version. The reason for that is that with the complementary logic configuration, a reference voltage is fixed at the non-inverting input of the comparator. Consequently, the comparator operates at this fixed threshold independent of the input voltage. For the straight binary configuration, the analog input drives the non-inverting input of the comparator so that the common mode voltage on the comparator input varies with the analog input. This adds a non-linear offset voltage of less than ¼ LSB.

Regardless which configuration is used, the comparator input common mode range must not be exceeded. In fact, the voltage at either comparator input must be no less than 0.5 volts from the negative supply and 2.0 volts from the positive supply. Therefore, for applications requiring common mode range to ground, simply connect a negative supply (−2V to −15V) to pin 20.

Layout Considerations

High resolution D/A and A/D converter circuits may have their entire error budget blown if any digital noise is allowed to enter the analog circuit.

Exercising care in the layout is certain to minimize frustrations. Single point analog grounding is a good place to start. All analog ground connections and supply bypassing should be returned to this point. In fact, in critical applications, the ADC1210 GND pin should be made ''the'' reference node. Furthermore, one should separate the analog ground from the digital ground. Any excursion of switching spikes generated in the digital circuit is, to some degree, decoupled from the analog circuitry. *Figure 6* illustrates this. Of course, these two points are eventually tied together at the power supply/chassis common.

In addition to a good ground system, it is a good idea to keep digital signal traces as far apart from the analog input as is practical in order to avoid signal cross coupling.

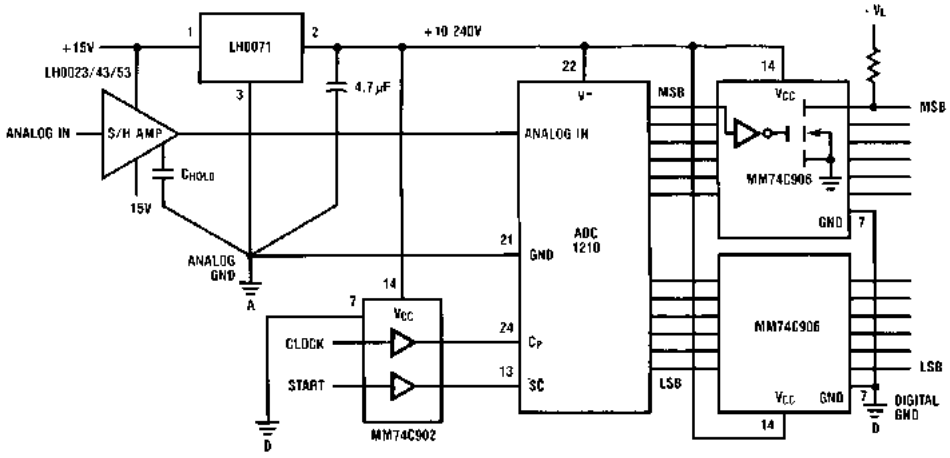

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FIGURE 6. Grounding Considerations of Interface Circuits

Power Supply Bypassing

The supply input only provides power to the digital logic, it is also a reference voltage to the resistor ladder network of the ADC1210. This voltage must be a very stable source. A precision reference device such as the LH0070 or LH0071 is ideal for the ADC1210. However, the internal CMOS Successive Approximation Register (SAR) invariably generates current spikes (10–20 mA peak) in the supply pin as the logic circuit switches past the linear region. Consequently, if a reference device such as the LH0070 is used, the current spike tends to cause excursions in the reference voltage, thus threatening conversion accuracy. To preserve the 12-bit accuracy, bypass the supply pin with a 4.7 μF tantalum capacitor. In high noise environments, a 22 μF capacitor shunted by a 0.1 μF ceramic disc capacitor is desirable.

If pin 20 is connected to a negative supply, it too should be bypassed to prevent voltage fluctuations from affecting the comparator operation.

Output Drive Capability

The digital outputs of the ADC1210 and the outputs of the SAR, through which the resistor ladder is referenced, are one and the same. Any excessive load current on the digital output lines will degrade conversion accuracy. For this reason, the ADC1210 must interface with CMOS logic. However, the three most significant bits (pins 10, 11, and 12) are buffered from the R-2R ladder and are capable of driving light loads without degrading linearity. This could prove useful in 2's complement applications where an inverter is necessary in the MSB; one might construct this inverter with a discrete NPN transistor and two resistors. The bit most sensitive to output loading is the fourth most significant (pin 9). An error voltage at this pin gets divided down by a factor of 16 before being applied to the comparator, so if we wish to limit the error due to output loading to say, ½ LSB, or 1.25 mV at the comparator, we can tolerate 20 mV at pin 9. If all lower bits will have the same output load, the error must be limited to 10 mV. Since all of the digital outputs have a maximum ON resistance of ç50Ω at 10V V_{REF} in both high and low states, the maximum allowable load current is 10 mV/ç50Ω = 29 μA. This current requirement is easily satisfied with an MM74C914 or MM74C901 thru MM74C902 level translators for interface with logic levels different than V_{REF}.

Comparator Hysteresis

Even an ideal comparator can be expected to oscillate due to stray capacitive feedback if biased in the linear region. It is the normal operation of the SAR feedback loop to do just that . . . at least at or toward the end of the conversion cycle. For most applications, this oscillation is only a minor bother, as the SAR register would have locked out the converted data from further changes at the end of conversion. If that is still undesirable, the Conversion Complete ($\overline{CC}$) Signal may be used to drive an open-collector gate (such as the MM74C906) with the output wire-ORed to the comparator output. In this way, the comparator is always clamped to the low state at the end of conversion. Normal operation resumes upon restart of a new conversion cycle.

In normal operation, however, if we want to preserve 12-bit accuracy, the comparator oscillation should be suppressed. The recommended technique is to apply a slight amount of AC hysteresis (50 mV) at the beginning of the decision cycle, but let it decay away to an acceptable accuracy before the decision is actually recorded in the SAR. The approximate decay time is (5) × (10k + 1k) × (100 pF), or 5.5 μs (see *Figure 2*).

For those applications using supply voltage other than 10V, say 5V, and if 50 mV initial hysteresis is to be maintained, the 200 kΩ (R_A) resistor in *Figure 2* should be changed to 100 kΩ based on the relationship:

$$\frac{R_B}{R_A + R_B} V_{REF} = 50 \text{ mV}$$

Where: R_B = 1 kΩ

High Speed Conversion Technique

By using one IC, one discrete NPN transistor, and a resistor, the ADC1210 can be made to run at up to 500 kHz clock frequency, or 12-bit conversion time of 26 μs. The circuit is shown in *Figure 7*. The idea is to clamp the comparator output low until the SAR is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions. This technique eliminates the need for the AC hysteresis circuit.

To implement the idea, a complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The inverted clock, generated from the same clock signal, is inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in working order. During the last half cycle, the comparator output is unclamped. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propagation delay such that the comparator output data is held long enough to resolve any internal logic set-up time requirements.

The 500 kHz clock implies that the absolute minimum amount of time required for the comparator output to be unclamped is 1 μs. Therefore, for applications with clock signal other than 50% duty cycle, this 1 μs period must be observed.

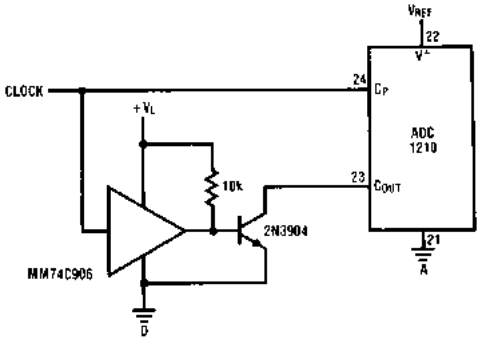

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FIGURE 7. High Speed Conversion Circuit

Testing has demonstrated reliable performance from this circuit beyond the recommended device operating frequency of 65 kHz. However, the AC hysteresis circuit is still a very reliable technique below this clock frequency and, therefore, should be used. Only in applications where the required clock frequency is above 65 kHz should the above-mentioned technique be adopted.

Synchronizing Conversion Start Signal

It is recommended that the $\overline{\text{START CONVERT}}$ input be synchronized to the CLOCK input. This avoids the possibility of the comparator making an error on the first (MSB) decision when the analog input is near ½ scale. There is a chance that energy can be coupled to the comparator from the rising edge of the $\overline{\text{START}}$ signal. If this occurs just before the rising edge of the clock, a wrong MSB decision can be made if time is not allowed for the charge to dissipate. The synchronization circuit in *Figure 8* effectively prevents this from occurring.

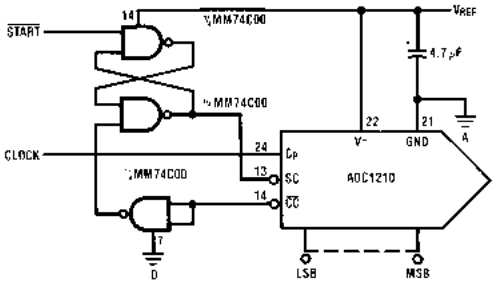

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FIGURE 8. Synchronizing START CONVERT Signal

The circuit operates as follows: initially the latch is in the RESET state and the converter is in the end-of-conversion state ($\overline{\text{CC}}$ output at logic low). The $\overline{\text{START}}$ signal sets the latch and, on the next positive clock transition, initializes all internal registers in the converter. The $\overline{\text{CC}}$ output is set to logic high, presetting the external latch. The latch is held in the "RESET" state during the entire conversion period, effectively preventing a new $\overline{\text{START}}$ signal from interrupting the conversion.

Serial Output

The comparator output does contain the stream of serially converted data with the most significant bit first. However, recognizing the danger of comparator oscillation, there is a potential for the external serial data register to latch a data bit different from that recorded in the SAR due to different logic set-up time requirements. If the ADC1210 accepts an error in any one data bit, the subsequent lower order bits tend to correct for it. On the other hand, an external serial register has no provision for error correction. All subsequent bits following a bit in error will not be valid data.

The 12 bits of information can be shifted out serially by using an MM74C150 digital multiplexer. The circuit is shown in *Figure 9*. This scheme permits valid data to be available at the serial output port as fast as half a clock cycle after the most current decision. The data are thus synchronized to the converter clock (here the serial data are synchronized at the falling edge of the system CLOCK, to avoid clock skew). Obviously, a number of variations can be made to this basic circuit for use with different handshake protocols.

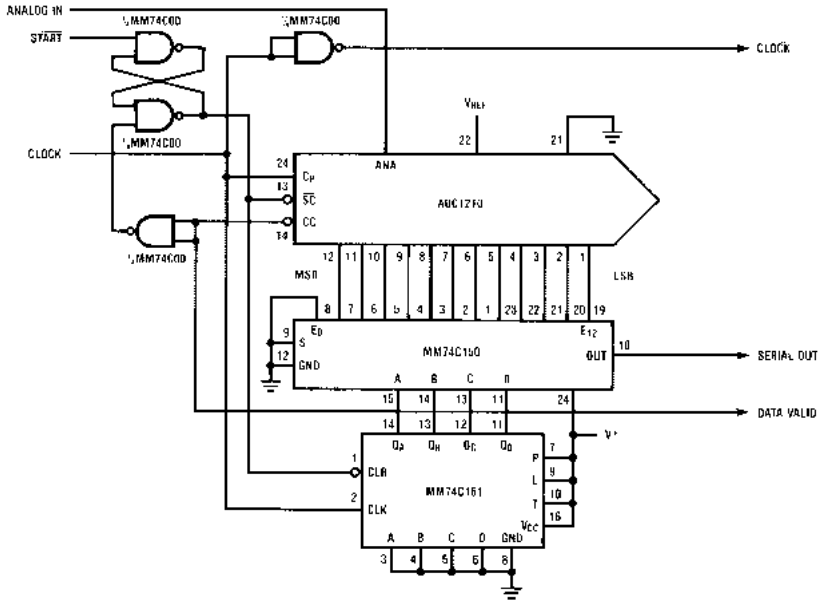

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FIGURE 9. 12-Bit A/D Converter with Serial Output

APPLICATIONS

Long Time Sample and Hold

The circuit in *Figure 10* is a particularly simple realization of an infinite sample and hold. This scheme requires two low-cost analog sample-and-hold amplifiers to complete the circuit.

The idea is to utilize the digital-loop feedback mechanism of the ADC1210 which, in the normal conversion mode, replicates the analog input voltage at the output of the SAR/D-to-A converter.

The operation of the circuit may be described as follows: During the normal ''hold'' mode, the replicated analog voltage is buffered straight through the S/H amplifier to the output. Upon an issuance of a $\overline{\text{SAMPLE}}$ signal, this S/H amplifier is placed in the hold mode, holding the voltage until the new analog voltage is valid. The same $\overline{\text{SAMPLE}}$ signal triggers an update to the input sample-and-hold amplifier. The most current analog voltage is captured and held for conversion. This way, the previously determined voltage is held stable at the output during the conversion cycle while the SAR/D-to-A continuously adjust to replicate the new input voltage. At the end of the conversion, the output sample-and-hold amplifier is once again placed in the track mode. The new analog voltage is then regenerated.

An Auto-Ranging Gain-Programmed A/D Converter

The circuit in *Figure 11* shows one possible circuit of an auto-ranging A/D converter. The circuit has a total of 8 gain ranges, with the ranging done in the LH0086 Programmable Gain Amplifier (for differential input, use the LH0084 with ranges of 1, 2, 5, 10 digitally programmed, or pin strap programmed for multiplying factors of 1, 4, and 10). The gain ranges are: 1, 2, 5, 10, 20, 50, 100, and 200. It effectively improves the A/D *resolution* from 12 bits to an equivalent of 19 bits, a dynamic range of better than 100 dB.

The circuit has relatively high speed ranging due to the very fast settling time of the LH0086, typically 5 μs for 10V swing, well within the 15 μs converter clock period. Thus, the ranging circuit is designed to work off the same clock.

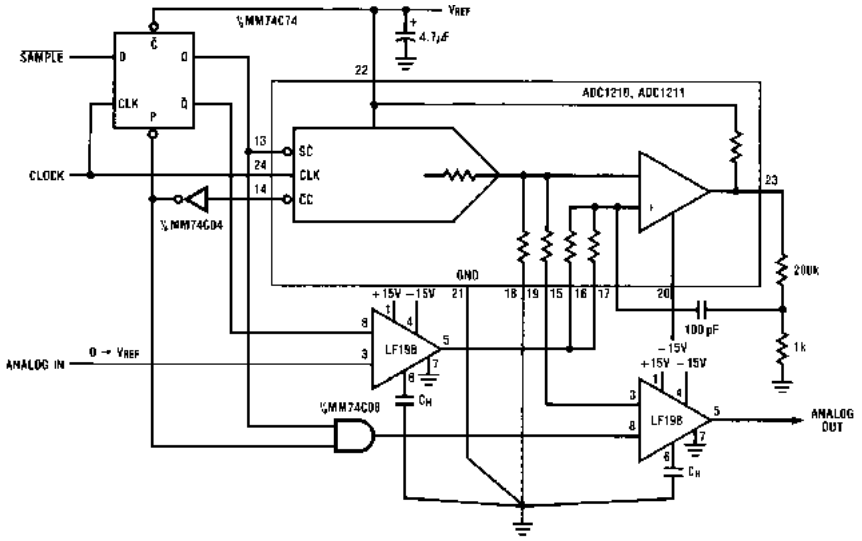
The circuit is designed such that the auto-ranging function is transparent to the user. All command signals into and out of the system are identical to those of an ADC1210 operating alone. The only exception is that the system requires one and one-half clock cycle (mandatory auto range cycle), plus however many ranges it has to scale to (each scale requires one clock period, 7 possible range switching in all) in addition to the basic 1ç conversion cycle required by the ADC1210. Therefore, in the best case where no ranging is necessary, the circuit adds 22.5 μs to the conversion time; and in the worst case, an additional 128 μs.

In the quiescent state where the ADC1210 is in the non-conversion mode, the auto-ranging circuit is free to function normally. Upon an issuance of a $\overline{\text{START}}$ signal, the next clock rising edge puts the circuit in the final auto range cycle before conversion begins. If the need for up-range or down-range is detected, the circuit remains in the auto range mode until all necessary scaling is completed. The control circuit then issues a start conversion signal to the ADC1210. Half a clock cycle later, the ADC1210 begins conversion and suspends the auto-ranging operation until the conversion is completed. At which time the 12-bit converter data plus the ç-bit range data are valid for further processing.

This design is suitable for applications in data-acquisition systems or portable instruments, particularly where low power is an important consideration. Other variations from this basic scheme can be realized depending on the user's requirements.

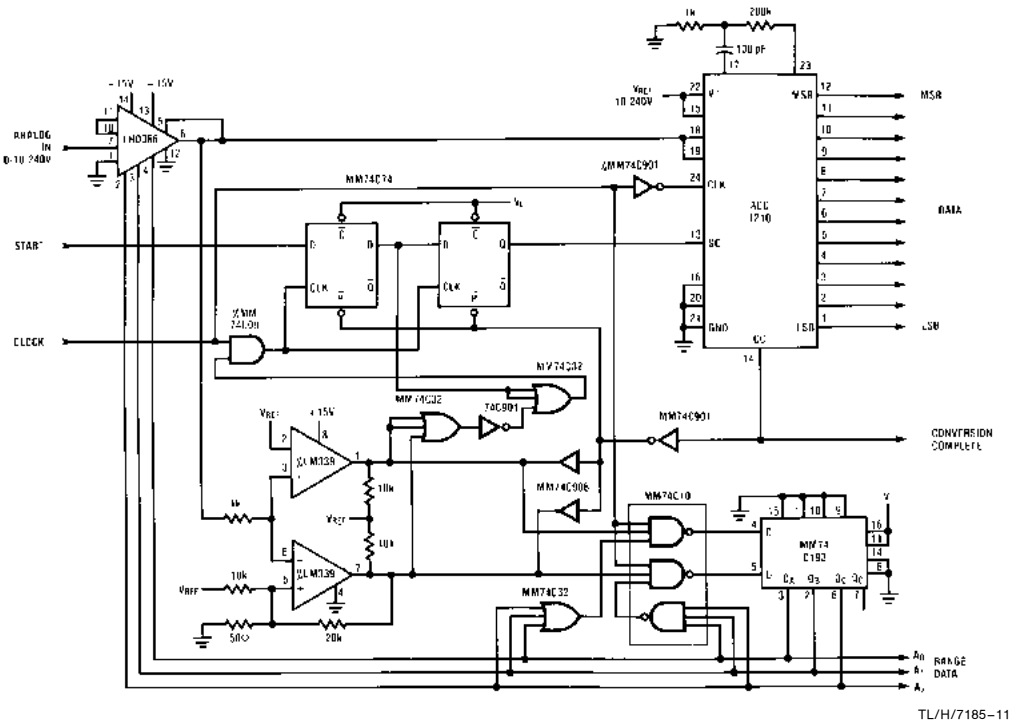
SUMMARY

The ADC1210 is a low-cost, medium-speed CMOS analog-to-digital converter with 12-bit resolution and linearity. It has wide supply range and flexible configuration to allow varied applications such as field instruments and sampled data systems.



TL/H/7185–10

FIGURE 10. Infinite Sample and Hold Amplifier



TL/H/7185–11

FIGURE 11. Auto Gain Ranging A/D Converter

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National Semiconductor

March 2006

ADC08161
500 ns A/D Converter with S/H Function and 2.5V Bandgap Reference

General Description

This product is on Lifetime Buy and is NOT RECOMMENDED for new designs.

Using a patented multi-step A/D conversion technique, the 8-bit ADC08161 CMOS A/D converter offers 500 ns conversion time, internal sample-and-hold (S/H), a 2.5V bandgap reference, and dissipates only 100 mW of power. The ADC08161 performs an 8-bit conversion with a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LBSs.

Input signals are tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold. The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to typically more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

For ease of interface to microprocessors, this part has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

- Resolution — 8 Bits
- Conversion time (t_{CONV}) — 560 ns max ($\overline{WR}$-$\overline{RD}$ Mode)
- Full power bandwidth — 300 kHz (typ)
- Throughput rate — 1.5 MHz min
- Power dissipation — 100 mW max
- Total unadjusted error — ±½ LSB and ±1 LSB max

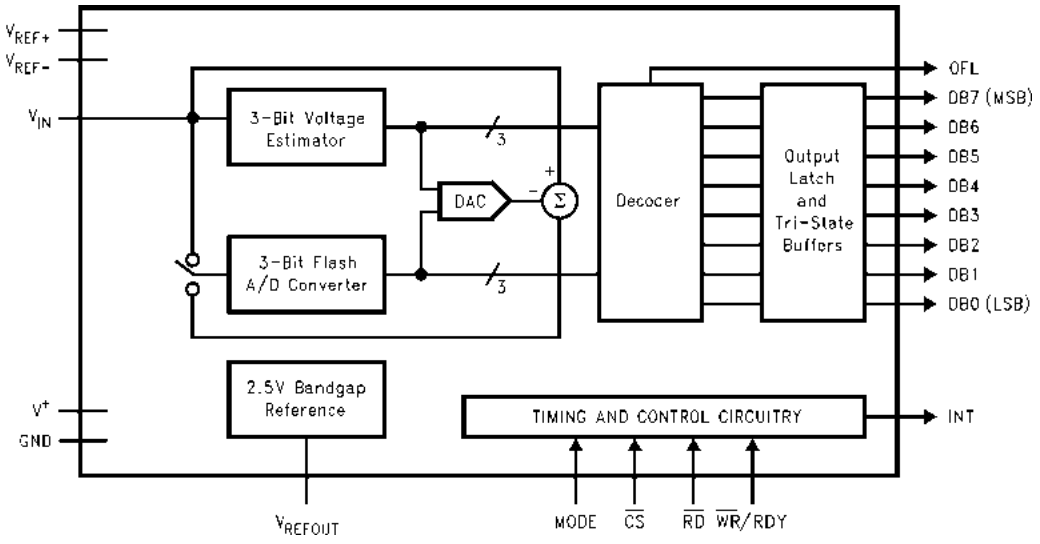
Features

- No external clock required
- Analog input voltage range from GND to V^+
- 2.5V bandgap reference

Applications

- Mobile telecommunications
- Hard-disk drives
- Instrumentation
- High-speed data acquisition systems

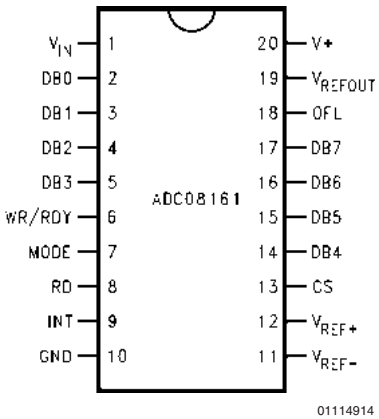
Block Diagram



TRI-STATE® is a trademark of National Semiconductor Corporation.

Connection Diagram

Wide-Body Small-Outline Package



See NS Package Number M20B

Ordering Information

Industrial ($-40^{\circ}C \le T_A \le 85^{\circ}C$)	Package
ADC08161CIWM	M20B

Pin Descriptions

V_{IN} This is the analog input. The input range is GND–50 mV ≤ V_{INPUT} ≤ V^+ + 50 mV.

DB0–DB7 TRI-STATE® data outputs—bit 0 (LSB) through bit 7 (MSB).

$\overline{WR}$ /RDY **$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin)

$\overline{WR}$: With $\overline{CS}$ low, the conversion is started on the rising edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (*Figures 2, 3, 4*).

$\overline{RD}$ Mode (Logic low applied to MODE pin)

RDY: This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$ and returns high at the end of conversion.

MODE **Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$**) selection input– This pin is pulled to a logic low through an internal 50 µA current sink when left unconnected.

$\overline{RD}$ Mode is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears.

$\overline{WR}$-$\overline{RD}$ Mode is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data.

$\overline{RD}$ **$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin)

This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (*Figures 2, 3, 4*).

$\overline{RD}$ Mode (logic low on the MODE pin)

With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion (*Figures 1, 5*).

$\overline{INT}$ This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$.

GND This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.

V_{REF-}, V_{REF+} These are the reference voltage inputs. They may be placed at any voltage between GND – 50 mV and V^+ + 50 mV, but V_{REF+} must be greater than V_{REF-}. Ideally, an input voltage equal to V_{REF-} produces an output code of 0, and an input voltage greater than V_{REF+} – 1.5 LSB produces an output code of 255.

For the ADC08161 an input voltage that exceeds V^+ by more than 100 mV or is below GND by more than 100 mV will create conversion errors.

$\overline{CS}$ This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals.

$\overline{OFL}$ Overflow Output. If the analog input is higher than V_{REF+}, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08161s to achieve higher resolution (9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read.

V^+ Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 µF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible.

V_{REFOUT} The internal bandgap reference's 2.5V output is available on this pin. Use a 220 µF bypass capacitor between this pin and analog ground.

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V^+)	6V
Logic Control Inputs	−0.3V to V^+ + 0.3V
Voltage at Other Inputs and Outputs	−0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	875 mW
Lead Temperature (Note 5)	
(Vapor Phase, 60 sec.)	+215˚C
(Infrared, 15 sec.)	+220˚C
Storage Temperature	−65˚C to +150˚C
ESD Susceptibility (Note 6)	750V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08161CIWM	$-40˚C \le T_A \le 85˚C$
Supply Voltage, (V^+)	4.5V to 5.5V

This product is on Lifetime Buy and NOT recommended for new designs.

Converter Characteristics

The following specifications apply for $\overline{RD}$ Mode, $V^+ = 5V$, $V_{REF+} = 5V$, and V_{REF-} = GND unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25˚C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
INL	Integral Non Linearity	$V_{REF} = 5V$		**±1**	LSB (max)
TUE	Total Unadjusted Error (Note 9)	$V_{REF} = 5V$		**±1**	LSB (max)
INL	Integral Non Linearity	$V_{REF} = 2.5V$		**±1**	LSB (max)
TUE	Total Unadjusted Error	$V_{REF} = 2.5V$		**±1**	LSB (max)
	Missing Codes	$V_{REF} = 5V$		**0**	Bits (max)
		$V_{REF} = 2.5V$		**0**	Bits (max)
	Reference Input Resistance		700	**500**	Ω (min)
			700	**1250**	Ω (max)
V_{REF+}	Positive Reference Input Voltage			**V_{REF-}**	V (min)
				V^+	V (max)
V_{REF-}	Negative Reference Input Voltage			**GND**	V (min)
				V_{REF+}	V (max)
V_{IN}	Analog Input Voltage	(Note 10)		**GND − 0.1**	V (min)
				V^+ + 0.1	V (max)
	On-Channel Input Current	On Channel Input = 5V, Off Channel Input = 0V (Note 11)	−0.4	**−20**	µA (max)
		On Channel Input = 0V, Off Channel Input = 5V (Note 11)	−0.4	**−20**	µA (max)
PSS	Power Supply Sensitivity	All Codes Tested, $V_{REF} = 4.75V$, $V^+ = 5V$ ±5%,	±1/16	**±½**	LSB (max)
	Effective Bits	$V_{IN} = 4.85\ V_{p-p}$, f_{IN} = 20 Hz to 20 kHz	7.8		Bits
	Full-Power Bandwidth	$V_{IN} = 4.85\ V_{p-p}$	300		kHz
THD	Total Harmonic Distortion	$V_{IN} = 4.85\ V_{p-p}$, f_{IN} = 20 Hz to 20 kHz	0.5		%
S/N	Signal-to-Noise Ratio	$V_{IN} = 4.85\ V_{p-p}$, f_{IN} = 20 Hz to 20 kHz	50		dB
IMD	Intermodulation Distortion	$V_{IN} = 4.85\ V_{p-p}$ f_{IN} = 20 Hz to 20 kHz	50		dB
C_{VIN}	Analog Input Capacitance		25		pF

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $t_r = t_f = 10$ ns, $V_{REF+} = 5V$, $V_{REF-} = 0V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
$t_{\overline{WR}}$	Write Time	Mode Pin to V^+ (*Figures 2, 3, 4*)	100	**100**	ns (min)
$t_{\overline{RD}}$	Read Time (Time from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{RD}$)	Mode Pin to V^+, (*Figure 2*)	350	**350**	ns (min)
t_{RDW}	$\overline{RD}$ Width	Mode Pin to GND (*Figure 5*)	200 400	**250** **400**	ns (min) ns (max)
t_{CONV}	$\overline{WR}$ -$\overline{RD}$ Mode Conversion Time ($t_{WR} + t_{RD} + t_{ACC1}$)	Mode Pin to V^+, (*Figure 2*)	500	**560**	ns (max)
t_{CRD}	$\overline{RD}$ Mode Conversion Time	Mode Pin to GND, (*Figure 1*)	655	**900**	ns (max)
t_{ACCO}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \le 100$ pF, Mode Pin to GND (*Figure 1*)	640	**900**	ns (max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode Pin to V^+, $t_{RD} \le t_{INTL}$ (*Figure 2*) $C_L = 10$ pF $C_L \le 100$ pF	 45 50	 **110**	 ns ns (max)
		$t_{RD} > t_{INTL}$, (*Figures 3, 5*)			
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \le 10$ pF $C_L = 100$ pF	25 30	 **55**	ns ns (max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$R_L = 3$ kΩ, $C_L = 10$ pF (*Figures 1, 2, 3, 4, 5*)	30	**60**	ns (max)
$t_{\overline{INTL}}$	Delay from Rising Edge of$\overline{WR}$ to Falling Edge of $\overline{INT}$	Mode Pin = V^+, $C_L = 50$ pF (*Figures 3, 4*)	520	**690**	ns (max)
$t_{\overline{INTH}}$	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF, (*Figures 1, 2, 3, 5*)	50	**95**	ns (max)
$t_{\overline{INTH}}$	Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF, (*Figure 4*)	45	**95**	ns (max)
t_{RDY}	Delay from $\overline{CS}$ to RDY	Mode Pin = 0V, $C_L = 50$ pF, $R_L = 3$ kΩ, (*Figure 1*)	25	**45**	ns (max)
t_{ID}	Delay from $\overline{INT}$ to Output Valid	$R_L = 3$ kΩ, $C_L = 100$ pF (*Figure 4*)	0	**15**	ns (max)
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$	Mode Pin = V^+, $t_{RD} \le t_{INTL}$ (*Figure 2*)	60	**115**	ns (max)
t_N	Time between End of $\overline{RD}$ and Start of New Conversion	(*Figures 1, 2, 3, 4, 5*)	50	**50**	ns (min)
$t_{\overline{CSS}}$	$\overline{CS}$ Setup Time	(*Figures 1, 2, 3, 4, 5*)	0	**0**	ns (max)
$t_{\overline{CSH}}$	$\overline{CS}$ Hold Time	(*Figures 1, 2, 3, 4, 5*)	0	**0**	ns (max)

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
V_{IH}	Logic “1” Input Voltage	$V^+ = 5.5$ V $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins Mode Pin		 **2.0** **3.5**	 V (min)

DC Electrical Characteristics (Continued)

The following specifications apply for V^+ = 5V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
V_{IL}	Logic "0" Input Voltage	V^+ = 4.5V $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins Mode Pin		**0.8** **1.5**	V (max)
I_{IH}	Logic "1" Input Current	V_H = 5V $\overline{CS}$, $\overline{RD}$, A0, A, A2 Pins $\overline{WR}$ Pin Mode Pin	0.005 0.1 50	**1** **3** **200**	µA (max)
I_{IL}	Logic "0" Input Current	V_L = 0V $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, A1, A2 Mode Pins	–0.005	–2	µA (max)
V_{OH}	Logic "1" Output Voltage	V^+ = 4.75V I_{OUT} = –360 µA DB0–DB7, $\overline{OFL}$, $\overline{INT}$ I_{OUT} = –10 µA DB0–DB7, $\overline{OFL}$, $\overline{INT}$		**2.4** **4.5**	V (min) V (min)
V_{OL}	Logic "0" Output Voltage	V^+ = 4.75V I_{OUT} = 1.6 mA DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		**0.4**	V (max)
I_O	TRI-STATE Output Current	V_{OUT} = 5.0V DB0–DB7, RDY V_{OUT} = 0V DB0–DB7, RDY	0.1 –0.1	**3** **–3**	µA (max) µA (max)
I_{SOURCE}	Output Source Current	V_{OUT} = 0V DB0–DB7, $\overline{OFL}$, $\overline{INT}$	–26	**–6**	mA (min)
I_{SINK}	Output Sink Current	V_{OUT} = 5V DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY	24	**7**	mA (min)
I_C	Supply Current	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0	11.5	**20**	mA (max)
C_{OUT}	Logic Output Capacitance		5		pF
C_{IN}	Logic Input Capacitance		5		pF

Bandgap Reference Electrical Characteristics

The following specifications apply for V^+ = 5V unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
V_{REFOUT}	Internal Reference Output Voltage			**2.5 ± 2.0%**	V (max)
$\Delta V_{REF}/\Delta T$	Internal Reference Temperature Coefficient		40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Internal Reference Load Regulation	Sourcing ($0 \le I_L \le +10$ mA)	0.01	**0.1**	%/mA (max)
	Line Regulation	$4.75V \le V^+ \le 5.25V$	0.5	**6.0**	mV (max)
I_{SC}	Short Circuit Current	V_{REV} = 0V	35		mA (max)
$\Delta V_{REF}/\Delta_t$	Long Term Stability		200		ppm/kHr
	Start-Up Time	V^+: 0V→5V, C_L = 220 µF	40		ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Bandgap Reference Electrical Characteristics (Continued)

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltage (V_{IN} < GND or V_{IN} > V^+), the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current specification limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 4: The power dissipation of this device under normal operation should never exceed 875 mW (Quiescent Power Dissipation + TTL Loads on the digital outputs). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (e.g., when any input or output exceeds the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 105˚C and θ_{JA} = 85˚C/W.

Note 5: See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at 25˚C and represent most likely parametric norm.

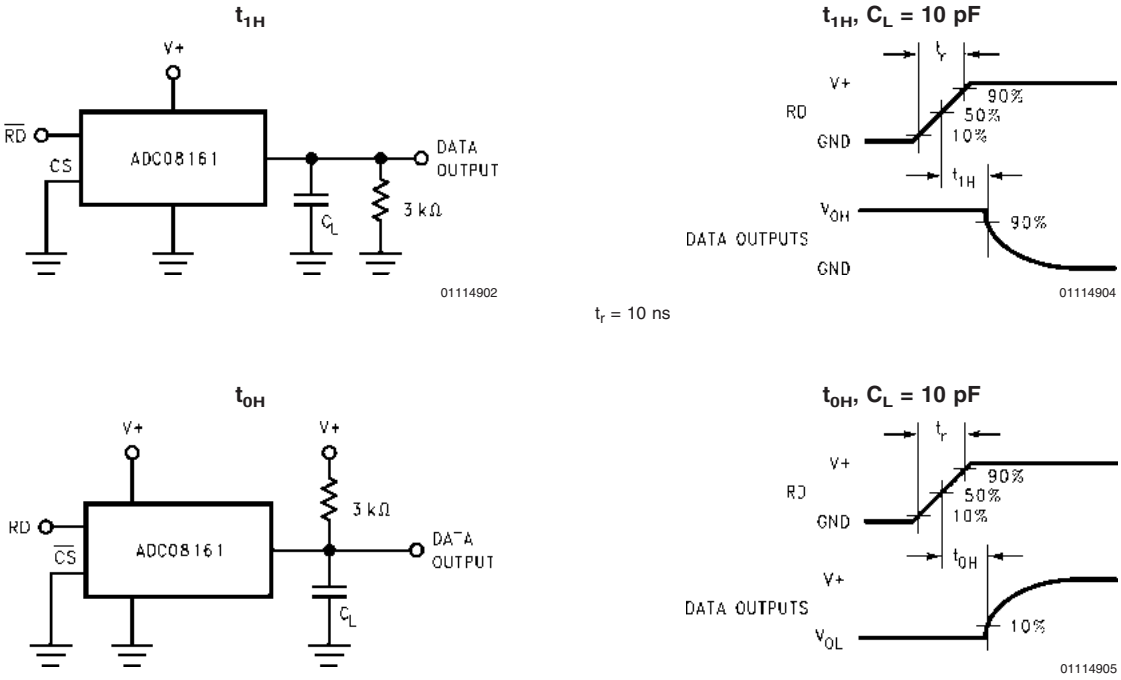
Note 8: Limits are guaranteed to National’s AOQL (Average Output Quality Level).

Note 9: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 10: Two on-chip diodes are tied to each analog input and are reversed biased during normal operation. One is connected to V^+ and the other is connected to GND. They will become forward biased and conduct when an analog input voltage is equal to or greater than one diode drop above V^+ or below GND. Therefore, caution should be exercised when testing with V^+ = 4.5V. Analog inputs with magnitudes equal to 5V can cause an input diode to conduct, especially at elevated temperatures. This can create conversion errors for analog signals near full-scale. The specification allows 50 mV forward bias on either diode; e.g., the output code will be correct as long as the analog input signal does not exceed the supply voltage by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. An absolute analog input signal voltage range of $0V \leq V_{IN} \leq 5V$ can be achieved by ensuring that the minimum supply voltage applied to V^+ is 4.950V over temperature variations, initial tolerance, and loading.

Note 11: Off-channel leakage current is measured on the on-channel selection.

TRI-STATE Test Circuit and Waveforms



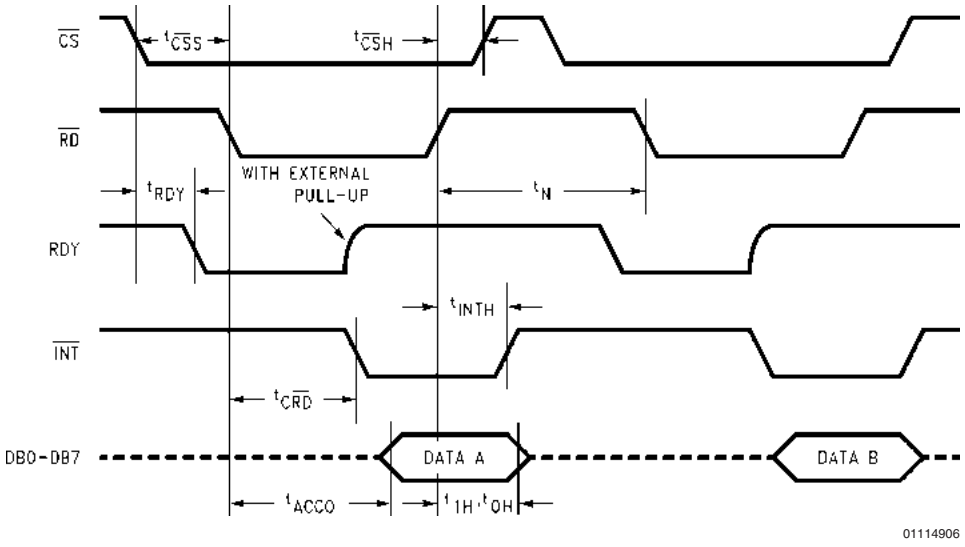


FIGURE 1. $\overline{RD}$ Mode (Mode Pin is Low)

TRI-STATE Test Circuit and Waveforms (Continued)

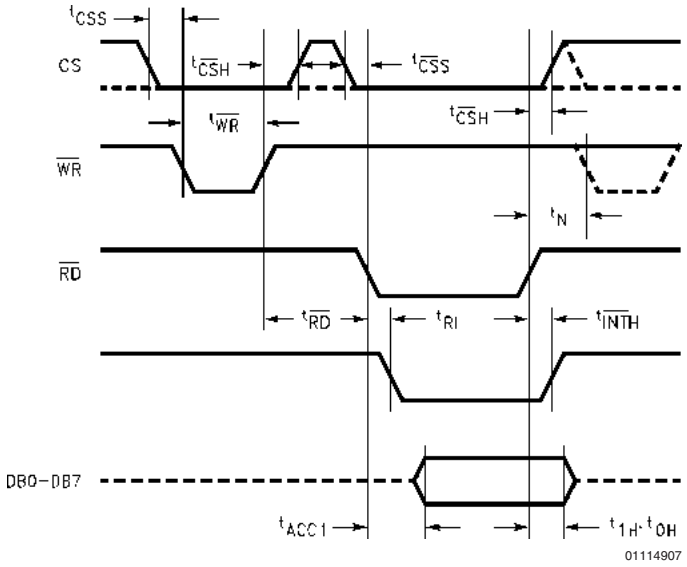


FIGURE 2. $\overline{WR}$-$\overline{RD}$ Mode with $t_{RD} \leq t_{INTL}$ (Mode Pin is High)

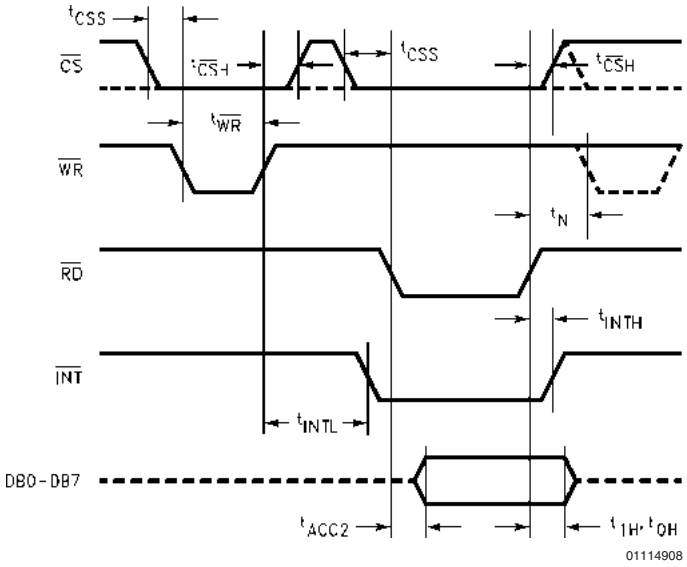


FIGURE 3. $\overline{WR}$-$\overline{RD}$ Mode with $t_{RD} > t_{INTL}$ (Mode Pin is High)

TRI-STATE Test Circuit and Waveforms (Continued)

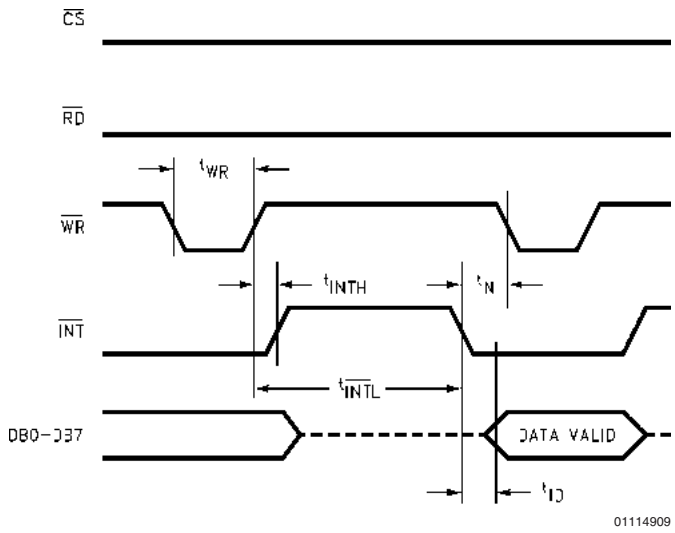


FIGURE 4. WR-RD Mode Reduced Interface System Connection with CS = RD = 0 (Mode Pin is High)

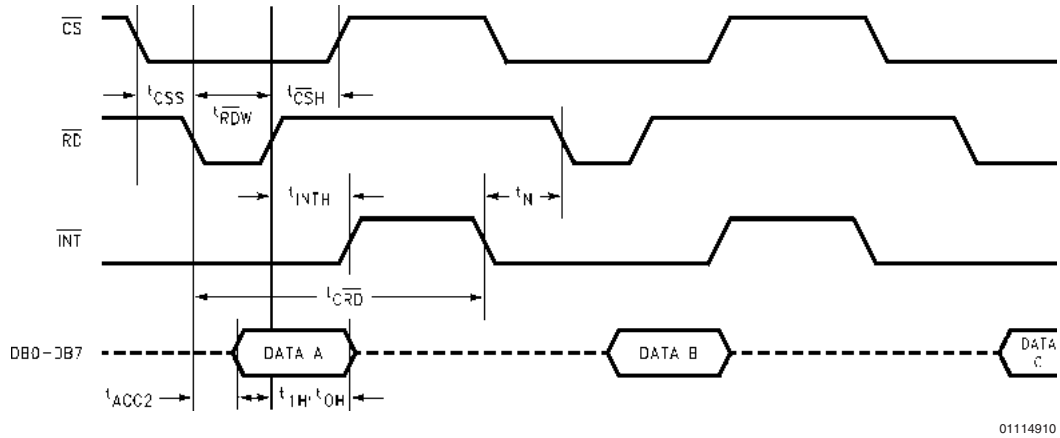
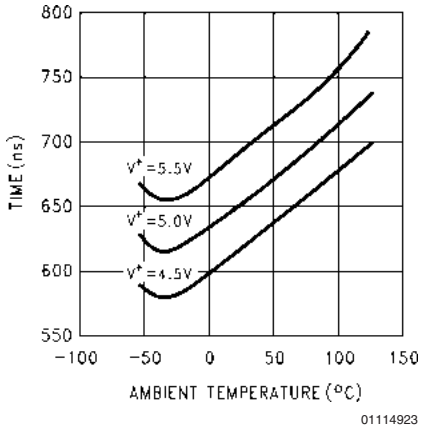


FIGURE 5. RD Mode (Pipeline Operation); t_{RDW} must be between 200 ns and 400 ns. (Mode Pin is Low)

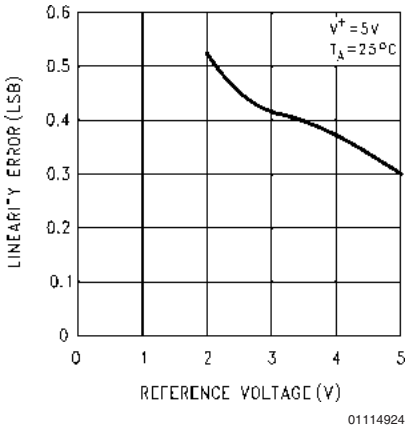
Typical Performance Characteristics

t_{CRD} vs Temperature



01114923

Linearity Error vs Reference Voltage



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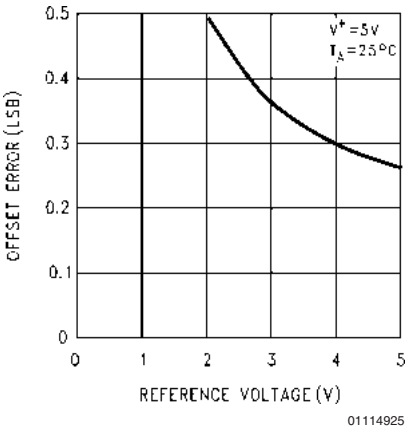
Offset Error vs Reference Voltage



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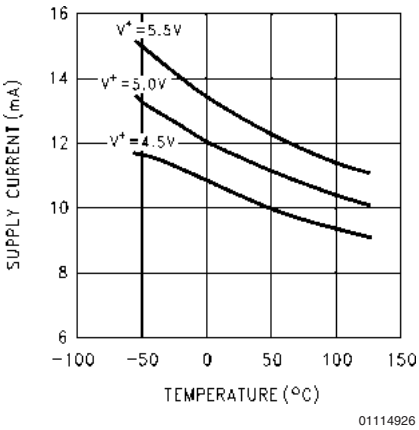
Supply Current vs Temperature



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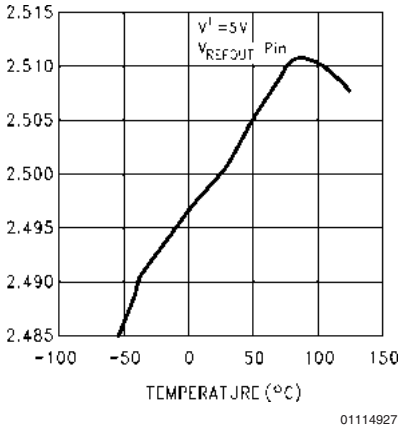
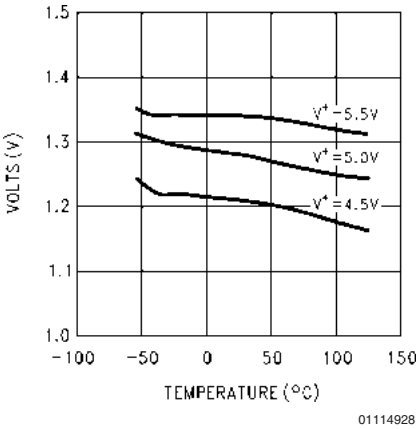
Reference Output Voltage vs Temperature



01114927

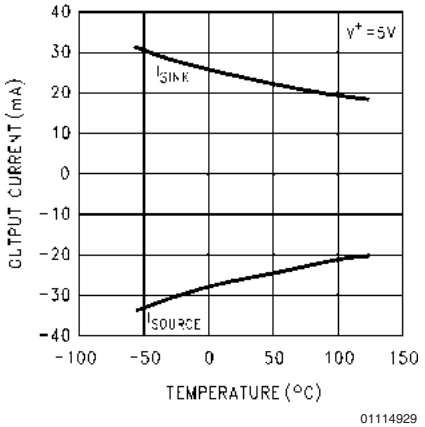
Logic Threshold vs Temperature



01114928

Typical Performance Characteristics (Continued)

Output Current vs Temperature



01114929

Application Information

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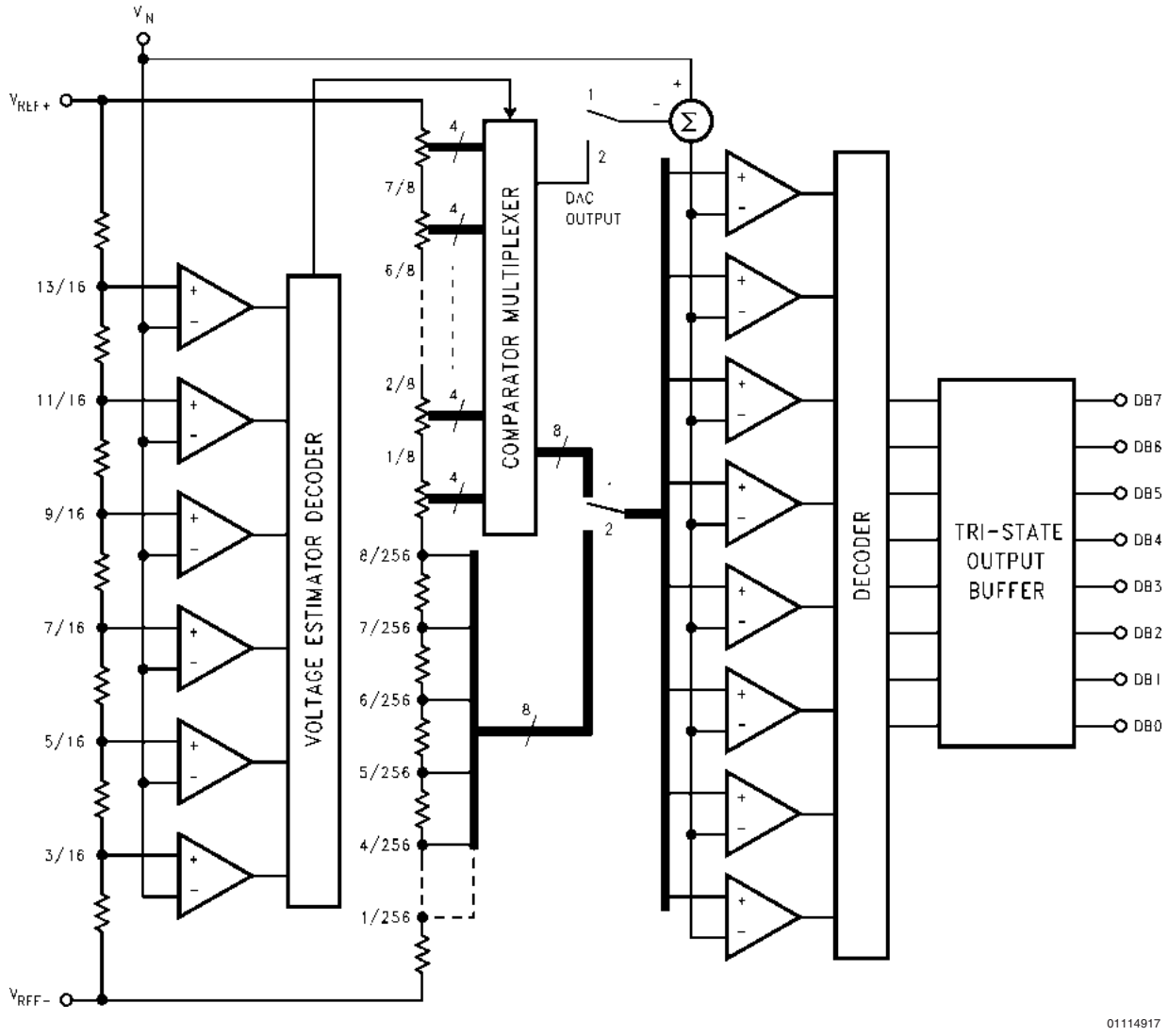


FIGURE 6. Block Diagram of the ADC08161 Multi-Step Flash Architecture

1.0 FUNCTIONAL DESCRIPTION

The ADC08161 performs an 8-bit analog-to-digital conversion using a multi-step flash technique. The first flash generates the five most significant bits (MSBs) and the second flash generates the three least significant bits (LSBs). *Figure 6* shows the major functional blocks of the ADC08161 multi-step flash converter. It consists of an over-encoded 2½-bit Voltage Estimator, an internal DAC with two different voltage spans, a 3-bit half-flash converter and a comparator multiplexer.

The resistor string near the center of the block diagram in *Figure 6* forms the internal main DAC. Each of the eight resistors at the bottom of the string is equal to 1/256 of the total string resistance. These resistors form the **LSB Ladder** and have a voltage drop of 1/256 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remaining resistors make up the **MSB Ladder** . They are made up of eight groups of four resistors connected in series. Each MSB Ladder section has ⅛ of the total reference voltage across it. Within a given MSB Ladder section, each of the MSB resistors has 8/256, or ⅓2 of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB Ladders. Through the Comparator Multiplexer these tap points can be connected, in groups of eight, to the eight comparators shown at the right of *Figure 6*. This function provides the necessary reference voltages to the comparators during each flash conversion.

The six comparators, seven-resistor string (estimator DAC), and Estimator Decoder at the left of *Figure 6* form the Voltage Estimator. The estimator DAC connected between V_{REF+} and V_{REF-} generates the reference voltages for the six Voltage Estimator comparators. These comparators perform a very low resolution A/D conversion to obtain an “estimate” of the input voltage. This estimate is then used to

Application Information **This product is on Lifetime Buy and NOT recommended for new designs.** (Continued)

control the Comparator Multiplexer, connecting the appropriate MSB Ladder section to the eight flash comparators. Only 14 comparators, six in the Voltage Estimator and eight in the flash converter, are needed to achieve the full eight-bit resolution, instead of 32 comparators that would be needed by traditional half-flash methods.

A conversion begins with the Voltage Estimator comparing the analog input signal against the six tap voltages on the estimator DAC. The estimator decoder then selects one of the groups of tap points along the MSB Ladder. These eight tap points are then connected to the eight flash comparators. For example, if the analog input signal applied to V_{IN} is between 0 and 3/16 of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the eight tap points between 8/256 and 2/8 of V_{REF} and connects them to the eight flash comparators. The first flash conversion is now performed, producing the five MSBs of data.

The remaining three LSBs are generated next using the same eight comparators that were used for the first flash conversion. As determined by the results of the MSB flash, a voltage from the MSB Ladder equivalent to the magnitude of the five MSBs is subtracted from the analog input voltage as the upper switch is moved from position one to position two. The resulting remainder voltage is applied to the eight flash comparators and, with the lower switch in position two, compared with the eight tap points from the LSB Ladder.

By using the same eight comparators for both flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard half-flash techniques.

Voltage Estimator errors as large as 1/16 of V_{REF}(16 LSBs) will be corrected since the flash comparators are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if 7/16 $V_{REF} < V_{IN} <$ 9/16 V_{REF} the Voltage Estimator's comparators tied to the tap points below 9/16 V_{REF} will output "1"s (000111). This is decoded by the estimator decoder to "10". The eight flash comparators will be placed at the MSB Ladder tap points between ⅜ V_{REF} and ⅝ V_{REF}. The overlap of 1/16 V_{REF} on each side of the Voltage Estimator's span will automatically correct an error of up to 16 LSBs (16 LSBs = 312.5 mV for V_{REF} = 5V). If the first flash conversion determines that the input voltage is between ⅜ V_{REF} and 4/8 V_{REF} − LSB/2, the Voltage Estimator's output code will be corrected by subtracting "1". This results in a corrected value of "01". If the first flash conversion determines that the input voltage is between 8/16 V_{REF} − LSB/2 and ⅝ V_{REF}, the Voltage Estimator's output code remains unchanged.

After correction, the 2-bit data from both the Voltage Estimator and the first flash conversion are decoded to produce the five MSBs. Decoding is similar to that of a 5-bit flash converter since there are 32 tap points on the MSB Ladder. However, 31 comparators are not needed since the Voltage Estimator places the eight comparators along the MSB Ladder where reference tap voltages are present that fall above and below the magnitude of V_{IN}. Comparators are not needed outside this selected range. If a comparator's output is a "0", all comparators above it will also have outputs of "0" and if a comparator's output is a "1", all comparators below it will also have outputs of "1".

2.0 DIGITAL INTERFACE

The ADC08161 has two basic interface modes which are selected by connecting the **MODE** pin to a logic high or low.

2.1 $\overline{RD}$ Mode

With a logic low applied to the **MODE** pin, the converter is set to **Read** mode. In this configuration (*Figure 1*), a complete conversion is done by pulling $\overline{RD}$ low, and holding low, until the conversion is complete and output data appears. This typically takes 655 ns. The $\overline{INT}$ (interrupt) line goes low at the end of conversion. A typical delay of 50 ns is needed between the rising edge of $\overline{CS}$ (after the end of a conversion) and the start of the next conversion (by pulling $\overline{RD}$ low). The RDY output goes low after the falling edge of $\overline{CS}$ and goes high at the end-of-conversion. It can be used to signal a processor that the converter is busy or serve as a system Transfer Acknowledge signal.

2.2 $\overline{RD}$ Mode Pipelined Operation

Applications that require shorter $\overline{RD}$ pulse widths than those used in the **Read** mode as described above can be achieved by setting $\overline{RD}$'s width between 200 ns–400 ns (*Figure 5*). $\overline{RD}$ pulse widths outside this range will create conversion linearity errors. These errors are caused by exercising internal interface logic circuitry using $\overline{CS}$ and/or $\overline{RD}$ during a conversion.

When $\overline{RD}$ goes low, a conversion is initiated and the data from the previous conversion is available on the DB0–DB7 outputs. Reading DB0–DB7 for the first two times after power-up produces random data. The data will be valid during the third $\overline{RD}$ pulse that occurs after the first conversion.

2.3 $\overline{WR}$-$\overline{RD}$ ($\overline{WR}$ then $\overline{RD}$) Mode

The ADC08161 is in the **$\overline{WR}$-$\overline{RD}$ mode** with the **MODE** pin tied high. A conversion starts on the rising edge of the $\overline{WR}$ signal. There are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for the $\overline{INT}$ output to go low before reading the conversion result (*Figure 3*). Typically, $\overline{INT}$ will go low 690 ns, maximum, after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 350 ns (*Figure 2*). If $\overline{RD}$ is pulled low before $\overline{INT}$ goes low, $\overline{INT}$ will immediately go low and data will appear at the outputs. This is the fastest operating mode ($t_{RD} \leq t_{INTL}$) with a conversion time, including data access time, of 560 ns. Allowing 100 ns for reading the conversion data and the delay between conversions gives a total throughput time of 660 ns (throughput rate of 1.5 MHz).

2.4 $\overline{WR}$-$\overline{RD}$ Mode with Reduced Interface System Connection

$\overline{CS}$ and $\overline{RD}$ can be tied low, using only $\overline{WR}$ to control the start of conversion for applications that require reduced digital interface while operating in the **$\overline{WR}$-$\overline{RD}$ mode** (*Figure 4*). Data will be valid approximately 705 ns following $\overline{WR}$'s rising edge.

3.0 REFERENCE INPUTS

The ADC08161's two V_{REF} inputs are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{REF+}$and V_{REF-}. Transducers that have outputs that minimum output voltages above GND can also

Application Information **This product is on Lifetime Buy and NOT recommended for new designs.** (Continued)

be compensated by connecting V_{REF-} to a voltage that is equal to this minimum voltage. By reducing V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$) to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF} = 2.5V, then 1 LSB = 9.8 mV). The reference arrangement also facilitates ratiometric operation and in may cases the power supply can be used for transducer power as well as the V_{REF} source. Ratiometric operation is achieved by connecting V_{REF-} to GND and connecting V_{REF+} and a transducer's power supply input to V^+. The ADC08161s accuracy degrades when $V_{REF+} - |V_{REF-}|$ is less than 2.0V.

The voltage at V_{REF-} sets the input level that produces a digital output of all zeroes. Through V_{IN} is not itself differential, the reference design affords nearly differential-input capability for some measurement applications. *Figure 7* shows one possible differential configuration.

It should be noted that, while the two V_{REF} inputs are fully differential, the digital output will be zero for any analog input voltage if $V_{REF-} \geq V_{REF+}$.

4.0 ANALOG INPUT AND SOURCE IMPEDANCE

The ADC08161's analog input circuitry includes an analog switch with an "on" resistance of 70Ω and a 1.4 pF capacitor (*Figure 7*). The switch is closed during the A/D's input signal acquisition time (while $\overline{WR}$ is low when using the $\overline{WR}$-$\overline{RD}$ Mode). A small transient current flows into the input pin each time the switch closes. A transient voltage, whose magnitude can increase as the source impedance increases, may be present at the input. So long as the source impedance is less than 500Ω, the input voltage transient will not cause errors and need not be filtered.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (100 ns maximum). A signal source with a high output impedance should have its output buffered with an operational amplifier. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Some suggested input configurations using the internal 2.5V reference, an external reference, and adjusting the input span are shown in *Figure 8*.

Correct conversion results will be obtained for input voltages greater than GND – 100 mV and less than V^+ + 100 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than V^+, or more than 300 mV lower than GND. The current flowing through any analog input pin should be limited to 5 mA or less to avoid permanent damage to the IC if an analog input pin is forced beyond these voltages. The sum of all the overdrive currents into all pins must be less than 20 mA. Some sort of protection scheme should be used when the input signal is expected to extend more than 300 mV beyond the power supply limits. A simple protection network using resistors and diodes is shown in *Figure 9*.

5.0 INHERENT SAMPLE-AND-HOLD

An important benefit of the ADC08161's input architecture is the inherent sample-and-hold (S/H) and its ability to measure relatively high speed signals without the help of an external S/H. In a non-sampling converter, regardless of its speed, the input must remain stable to at least ½ LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion.

The ADC08161 is suitable for DSP-based systems because of the direct control of the S/H through the $\overline{WR}$ signal. The $\overline{WR}$ input signal allows the A/D to be synchronized to a DSP system's sampling rate or to other ADC08161s.

The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

6.0 INTERNAL BANDGAP REFERENCE

The ADC08161 has an internal bandgap 2.5V reference that can be used as the V_{REF+} input. A parallel combination of a 0.1 µF ceramic capacitor and a 220 µF tantalum capacitor should be used to bypass the V_{REFOUT} pin. This reduces possible noise pickup that could cause conversion errors.

7.0 LAYOUT, GROUNDS, AND BYPASSING

In order to ensure fast, accurate conversions from the ADC08161, it is necessary to use appropriate circuit board layout techniques. Ideally, the analog-to-digital converter's ground reference should be low impedance and free of noise from other parts of the system. Digital circuits can produce a great deal of noise on their ground returns and, therefore, should have their own separate ground lines. Best performance is obtained using separate ground planes should be provided for the digital and analog parts of the system.

The analog inputs should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., an input filter capacitor) connected across the inputs should be returned to a very clean ground point. Incorrectly grounding the ADC08161 may result in reduced conversion accuracy.

The V^+ supply pin, V_{REF+}, and V_{REF-} (if not grounded) should be bypassed with a parallel combination of a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor placed as close as possible to the pins using short circuit board traces. See *Figures 8, 9*.

Application Information **This product is on Lifetime Buy and NOT recommended for new designs.** (Continued)

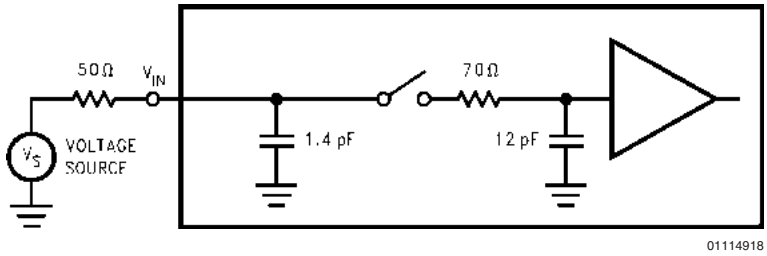
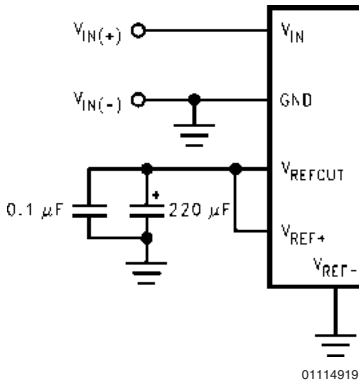
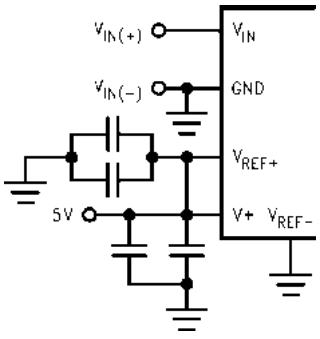


FIGURE 7. ADC08161 Equivalent Input Circuit Model

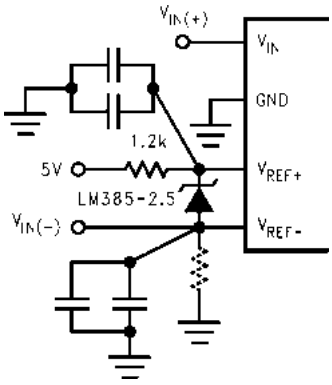
Internal Reference 2.5V Full-Scale (Standard Application)



Power Supply as Reference



Input Not Referred to GND



*Signal source driving $V_{IN}(-)$ must be capable of sinking 5 mA.

Note: Bypass capacitors consist of a 0.1 µF ceramic in parallel with a 10 µF bead tantalum, unless otherwise specified.

FIGURE 8. Analog Input Options

Application Information **This product is on Lifetime Buy and NOT recommended for new designs.** (Continued)

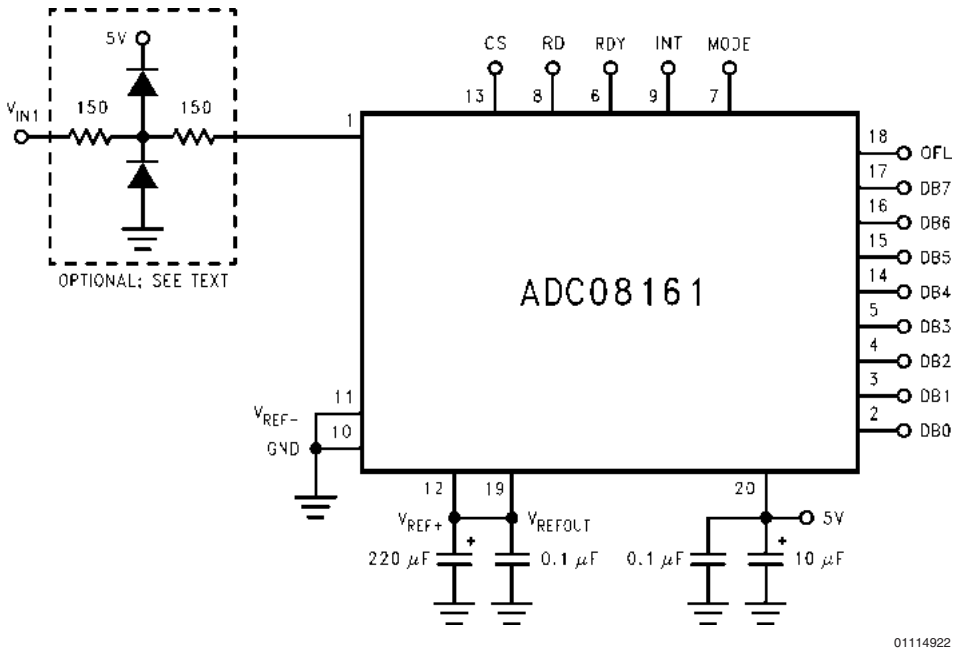
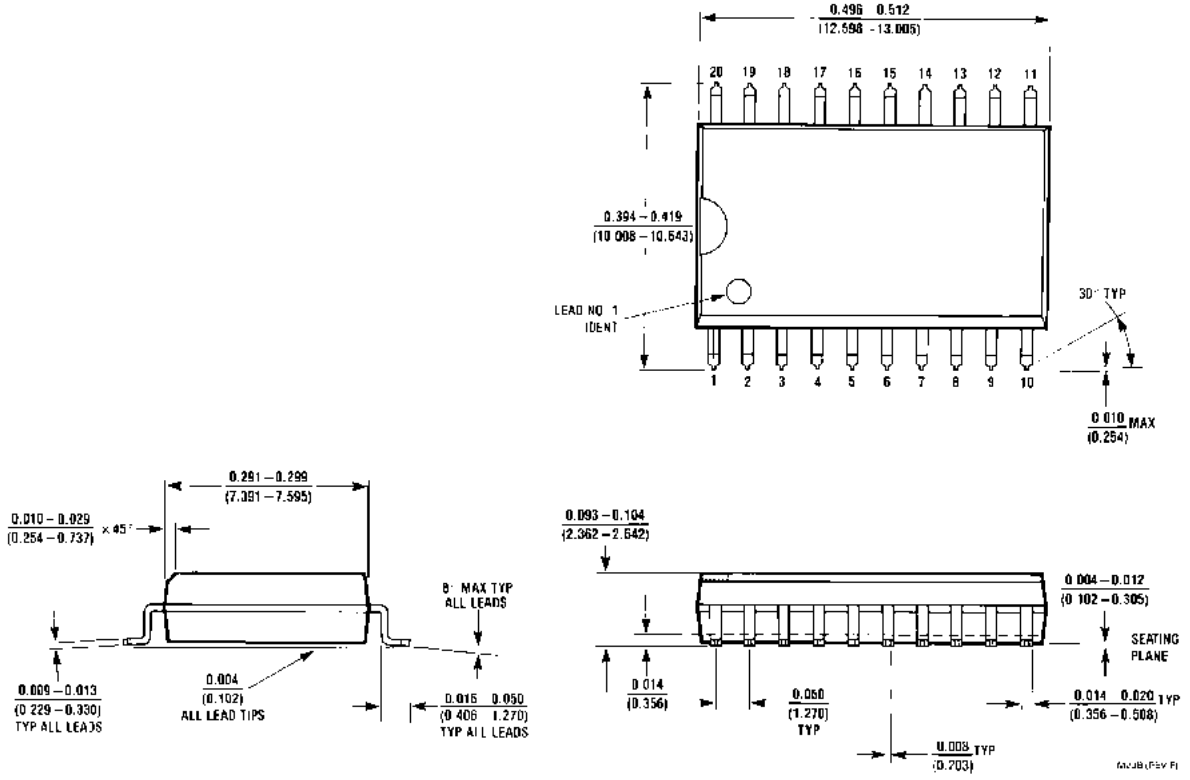


FIGURE 9. Typical Connection. Note the multiple bypass capacitors on the reference and power supply pins. V_{REF-} should be bypassed to analog ground using multiple capacitors if it is not grounded (See Section 7.0 "LAYOUT, GROUNDS, and BYPASSING"). V_{IN1} is shown with an optional input protection network.

Physical Dimensions inches (millimeters) unless otherwise noted



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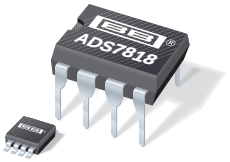

ADS7818

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12-Bit High Speed Low Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 500kHz THROUGHPUT RATE
- 2.5V INTERNAL REFERENCE
- LOW POWER: 11mW
- SINGLE SUPPLY +5V OPERATION
- DIFFERENTIAL INPUT
- SERIAL INTERFACE
- GUARANTEED NO MISSING CODES
- MINI-DIP-8 AND MSOP-8
- UNIPOLAR INPUT RANGE

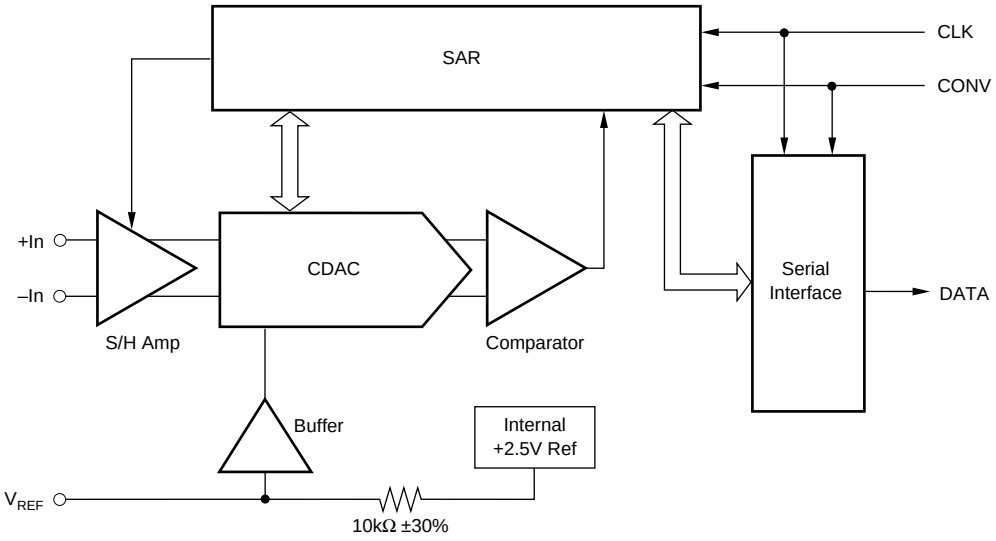
APPLICATIONS

- BATTERY OPERATED SYSTEMS
- DIGITAL SIGNAL PROCESSING
- HIGH SPEED DATA ACQUISITION
- WIRELESS COMMUNICATION SYSTEMS

DESCRIPTION

The ADS7818 is a 12-bit sampling analog-to-digital converter (A/D) complete with sample/hold, internal 2.5V reference, and synchronous serial interface. Typical power dissipation is 11mW at a 500kHz throughput rate. The device can be placed into a power down mode which reduces dissipation to just 2.5mW. The input range is zero to two times the reference voltage, and the internal reference can be overdriven by an external voltage.

Low power, small size, and high-speed make the ADS7818 ideal for battery operated systems such as wireless communication devices, portable multi-channel data loggers, and spectrum analyzers. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7818 is available in a plastic mini-DIP-8 or an MSOP-8 package and is guaranteed over the –40°C to +85°C temperature range.



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PDS-1408B
Printed in U.S.A. May, 2000
SBAS078

SPECIFICATIONS

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7818P, E			ADS7818PB, EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span[1]	+In – (–In)	0		5	*		*	V
Absolute Input Range	+In	–0.2		V_{CC} +0.2	*		*	V
	–In	–0.2		+0.2	*		*	V
Capacitance			15			*		pF
Leakage Current			1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			*			Bits
Integral Linearity Error			±1	±2		±0.5	±1	LSB[2]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error			±2	±5		±1	*	LSB
Gain Error[3]	25°C		±12	±30		±7	±15	LSB
	–40°C to +85°C			±50			±35	LSB
Common-Mode Rejection	DC, 0.2Vp-p		70			*		dB
	1MHz, 0.2Vp-p		50			*		dB
Noise			150			*		µVrms
Power Supply Rejection	Worst Case Δ, $+V_{CC}$ = 5V ±5%		1.2			*		LSB
SAMPLING DYNAMICS								
Conversion Time		1.625			*			µs
Acquisition Time		0.350			*			µs
Throughput Rate				500			*	kHz
Aperture Delay			5			*		ns
Aperture Jitter			30			*		ps
Step Response			350			*		ns
DYNAMIC CHARACTERISTICS								
Signal-to-Noise Ratio	V_{IN} = 5Vp-p at 100kHz		72			*		dB
Total Harmonic Distortion[4]	V_{IN} = 5Vp-p at 100kHz		–78	–72		–82	–75	dB
Signal-to-(Noise+Distortion)	V_{IN} = 5Vp-p at 100kHz	68	70		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 100kHz	72	78		75	82		dB
Usable Bandwidth	SINAD > 68dB		350			*		kHz
REFERENCE OUTPUT								
Voltage	I_{OUT} = 0	2.475	2.50	2.525	2.48	*	2.52	V
Source Current[5]	Static Load			50			*	µA
Drift	I_{OUT} = 0		20			*		ppm/°C
Line Regulation	4.75V ≤ V_{CC} ≤ 5.25V		0.6			*		mV
REFERENCE INPUT								
Range		2.0		2.55	*		*	V
Resistance[6]	to Internal Reference Voltage		10		*	*	*	kΩ
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels:								
V_{IH}	$\|I_{IH}\| \leq +5\mu A$	3.0		V_{CC} +0.3	*		*	V
V_{IL}	$\|I_{IL}\| \leq +5\mu A$	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = –500µA	3.5			*		*	V
V_{OL}	I_{OL} = 500µA			0.4	*		*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENT								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current	f_{SAMPLE} = 500kHz		2.2			*		mA
	Power Down		0.5			*		mA
Power Dissipation	f_{SAMPLE} = 500kHz		11	20		*	*	mW
	Power Down		2.5			*		mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as ADS7818P,E.

NOTES: (1) Ideal input span, does not include gain or offset error. (2) LSB means Least Significant Bit, with V_{REF} equal to +2.5V, one LSB is 1.22mV. (3) Measured relative to an ideal, full-scale input (+In – (–In)) of 4.999V. Thus, gain error includes the error of the internal voltage reference. (4) Calculated on the first nine harmonics of the input frequency. (5) If the internal reference is required to source current to an external load, the reference voltage will change due to the internal 10kΩ resistor. (6) Can vary ±30%.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to GND	–0.3V to 6V
Analog Inputs to GND	–0.3V to (V_{CC} + 0.3V)
Digital Inputs to GND	–0.3V to (V_{CC} + 0.3V)
Power Dissipation	325mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

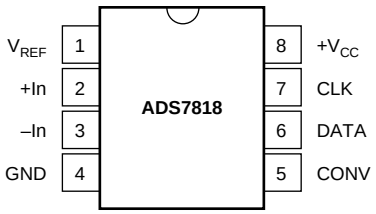
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

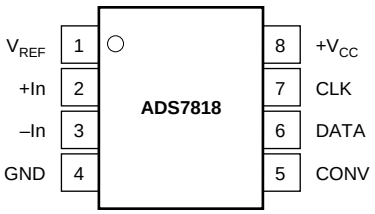
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View



Plastic Mini-DIP-8



MSOP-8

PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Output. Decouple to ground with a 0.1µF ceramic capacitor and a 2.2µF tantalum capacitor.
2	+In	Non-Inverting Input.
3	–In	Inverting Input. Connect to ground or to remote ground sense point.
4	GND	Ground.
5	CONV	Convert Input. Controls the sample/hold mode, start of conversion, start of serial data transfer, type of serial transfer, and power down mode. See the Digital Interface section for more information.
6	DATA	Serial Data Output. The 12-bit conversion result is serially transmitted most significant bit first with each bit valid on the rising edge of CLK. By properly controlling the CONV input, it is possibly to have the data transmitted least significant bit first. See the Digital Interface section for more information.
7	CLK	Clock Input. Synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	Power Supply. Decouple to ground with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor.

PACKAGE/ORDERING INFORMATION

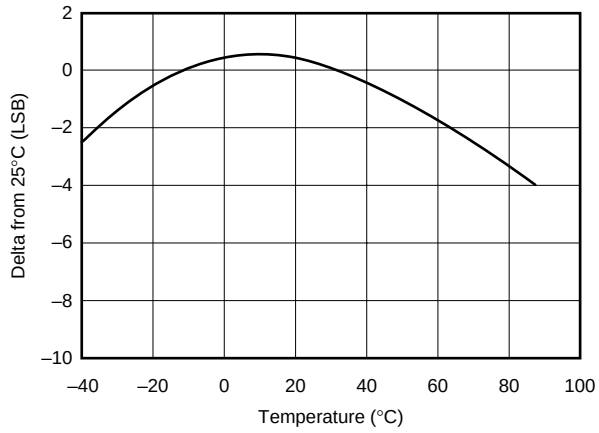
PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER(3)	TRANSPORT MEDIA
ADS7818E	±2	N/S(4)	MSOP-8	337	–40°C to +85°C	A18	ADS7818E/250	Tape and Reel
"	"	"	"	"	"	"	ADS7818E/2K5	Tape and Reel
ADS7818EB	±1	±1	MSOP-8	337	–40°C to +85°C	A18	ADS7818EB/250	Tape and Reel
"	"	"	"	"	"	"	ADS7818EB/2K5	Tape and Reel
ADS7818P	±2	N/S(4)	Plastic DIP-8	006	–40°C to +85°C	ADS7818P	ADS7818P	Rails
ADS7818PB	±1	±1	"	"	"	ADS7818PB	ADS7818PB	Rails

NOTE: (1) For detail drawing and dimension table, please see end of data sheet or Package Drawing File on Web. (2) Performance Grade information is marked on the reel. (3) Models with a slash(/) are available only in Tape and reel in quantities indicated (e.g. /250 indicates 250 units per reel, /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS7818E/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to the www.burr-brown.com web site under Applications and Tape and Reel Orientation and Dimensions. (4) N/S = Not Specified, typical only. However, 12-Bits no missing codes is guaranteed over temperature.

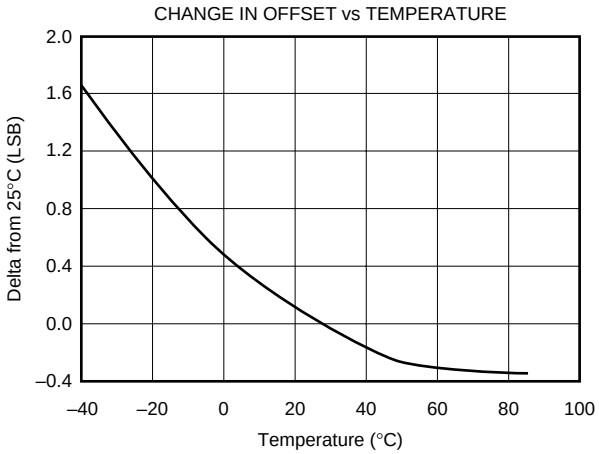
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal +2.5V reference, unless otherwise specified.

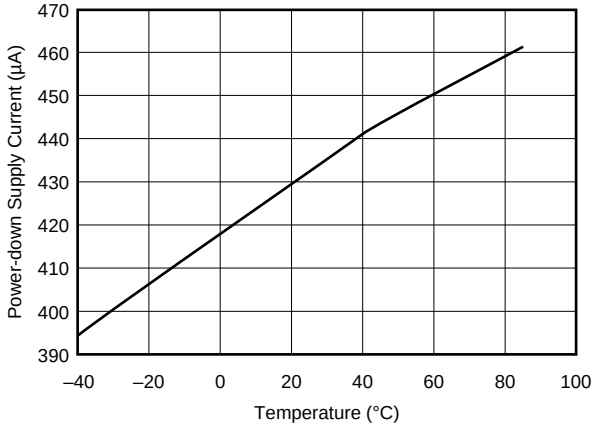
CHANGE IN FULL-SCALE ERROR vs TEMPERATURE



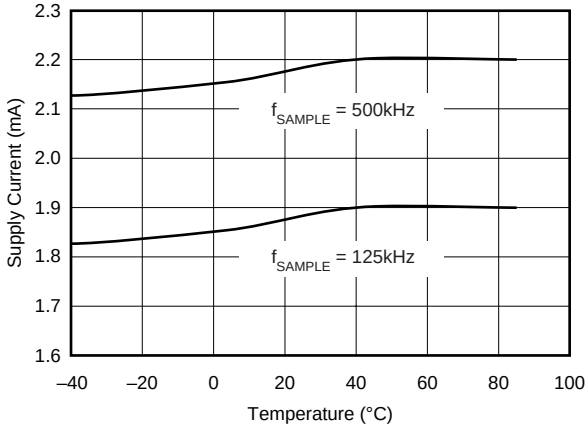
CHANGE IN OFFSET vs TEMPERATURE



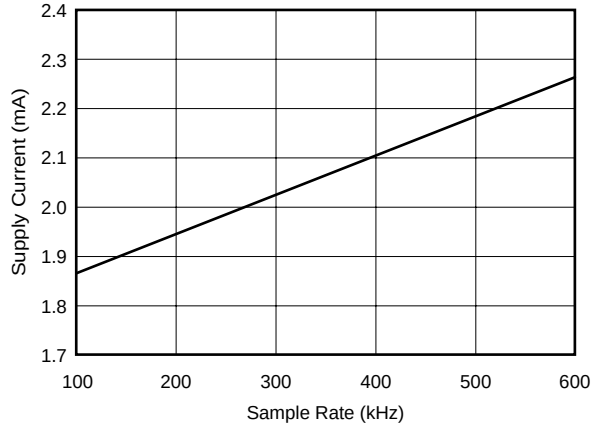
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



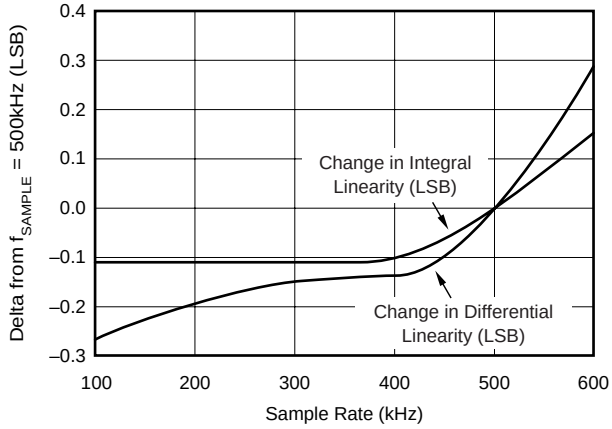
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SAMPLE RATE



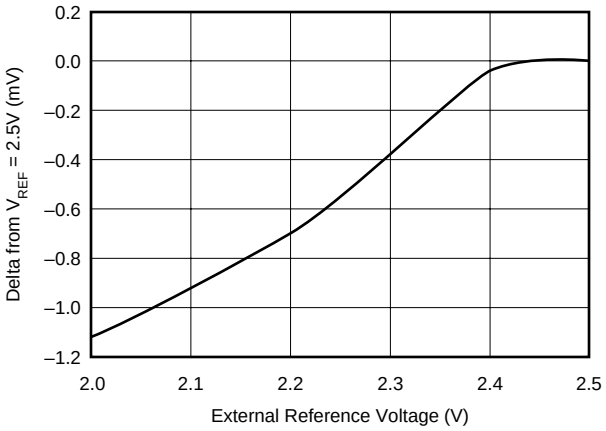
CHANGE IN INTEGRAL LINEARITY and DIFFERENTIAL LINEARITY vs SAMPLE RATE



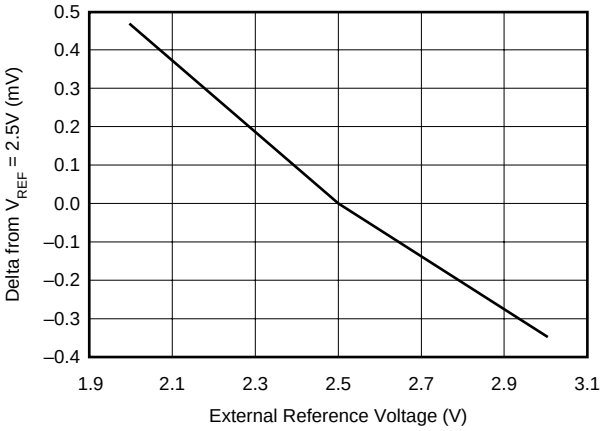
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{CC} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal +2.5V reference, unless otherwise specified.

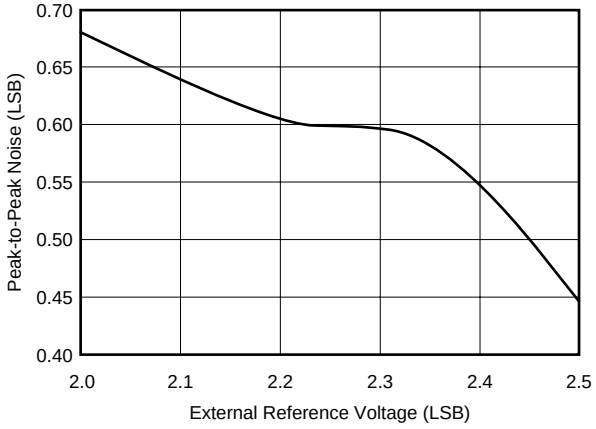
CHANGE IN FULL-SCALE ERROR
vs EXTERNAL REFERENCE VOLTAGE



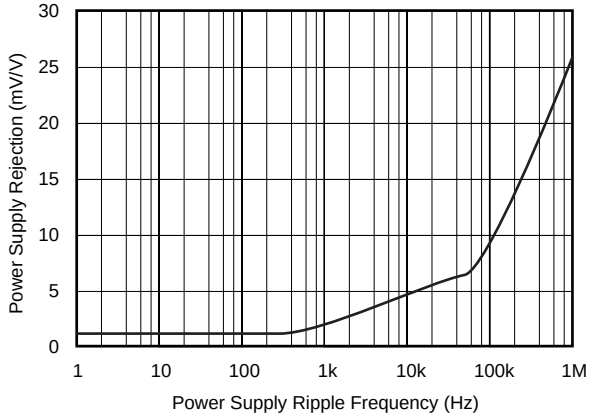
CHANGE IN OFFSET
vs EXTERNAL REFERENCE VOLTAGE



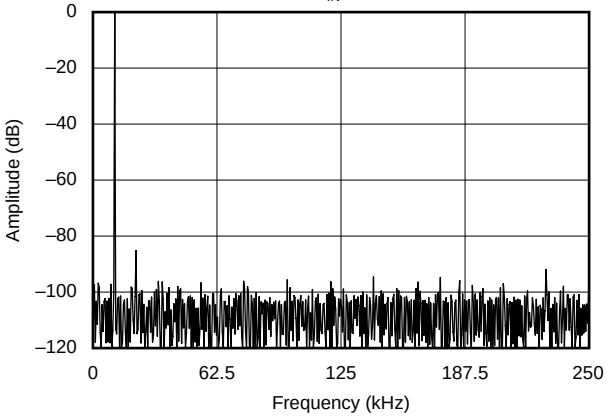
PEAK-TO-PEAK NOISE
vs EXTERNAL REFERENCE VOLTAGE



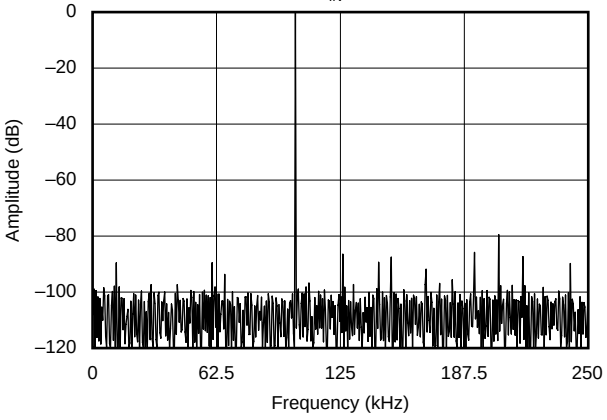
POWER SUPPLY REJECTION
vs POWER SUPPLY RIPPLE FREQUENCY



FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.9kHz, –0.2dB)



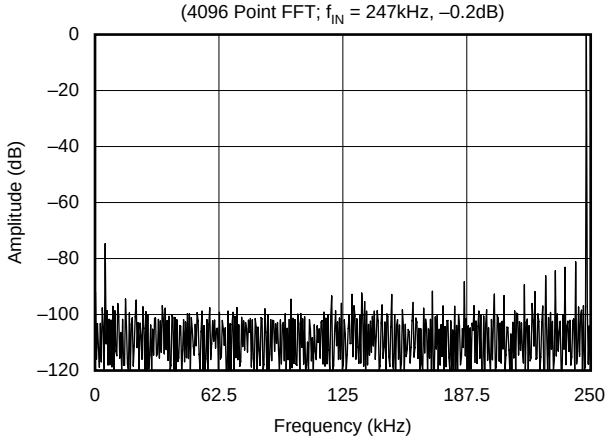
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 102kHz, –0.2dB)



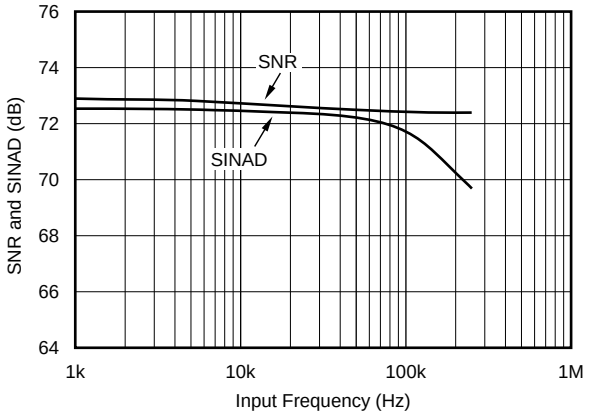
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{CC} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal +2.5V reference, unless otherwise specified.

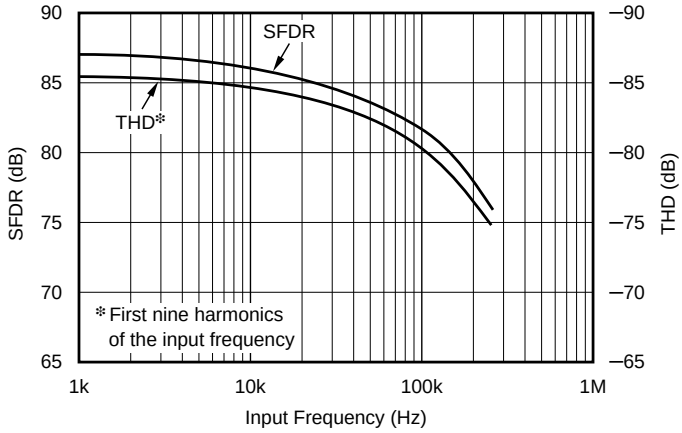
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 247kHz, –0.2dB)



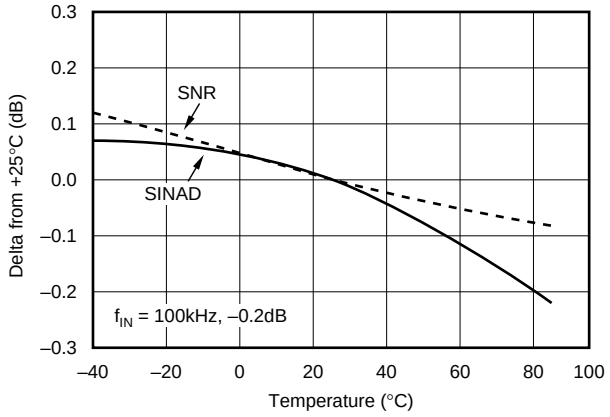
SIGNAL-TO-NOISE RATIO and
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY



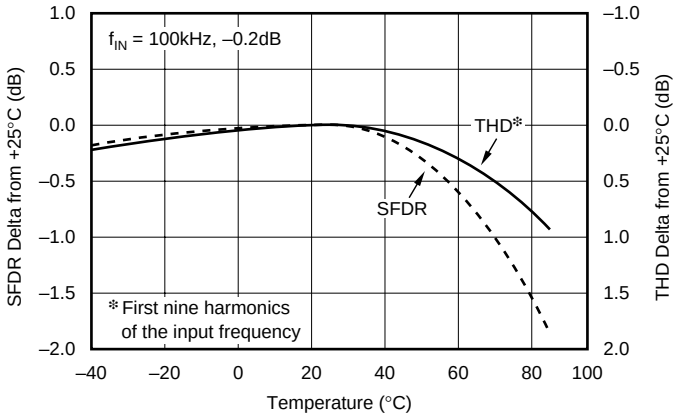
SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



CHANGE IN SIGNAL-TO-NOISE RATIO
and SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



CHANGE IN SPURIOUS FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs TEMPERATURE



THEORY OF OPERATION

The ADS7818 is a high speed successive approximation register (SAR) analog-to-digital converter (A/D) with an internal 2.5V bandgap reference. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. See Figure 1 for the basic operating circuit for the ADS7818.

The ADS7818 requires an external clock to run the conversion process. This clock can vary between 200kHz (12.5Hz throughput) and 8MHz (500kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 50ns and the clock period is at least 125ns. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7818.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The range of the analog input is set by the voltage on the V_{REF} pin. With the internal 2.5V reference, the input range is 0 to 5V. An external reference voltage can be placed on V_{REF}, overdriving the internal voltage. The range for the external voltage is 2.0V to 2.55V, giving an input voltage range of 4.0V to 5.1V.

The digital result of the conversion is provided in a serial manner, synchronous to the CLK input. The result is provided most significant bit first and represents the result of the conversion currently in progress—there is no pipeline delay. By properly controlling the CONV and CLK inputs, it is possible to obtain the digital result least significant bit first.

ANALOG INPUT

The +IN and –IN input pins allow for a differential input signal to be captured on the internal hold capacitor when the converter enters the hold mode. The voltage range on the –IN input is limited to –0.2V to 0.2V. Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the –IN input is best used to sense a remote ground point near the source of the +IN signal. If the source driving the +IN signal is nearby, the –IN should be connected directly to ground.

The input current into the analog input depends on input voltage and sample rate. Essentially, the current into the device must charge the internal hold capacitor during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the sample period—which can be as little as 350ns in some operating modes. While the converter is in the hold mode or after the sampling capacitor has been fully charged, the input impedance of the analog input is greater than 1GΩ.

Care must be taken regarding the input voltage on the +In and –IN pins. To maintain the linearity of the converter, the +In input should remain within the range of GND – 200mV to $+V_{CC}$ + 200mV. The –IN input should not drop below GND – 200mV or exceed GND + 200mV. Outside of these ranges, the converter's linearity may not meet specifications.

REFERENCE

The reference voltage on the V_{REF} pin directly sets the full-scale range of the analog input. The ADS7818 can operate with a reference in the range of 2.0V to 2.55V, for a full-scale range of 4.0V to 5.1V.

The voltage at the V_{REF} pin is internally buffered and this buffer drives the capacitor DAC portion of the converter. This is important because the buffer greatly reduces the dynamic load placed on the reference source. However, the voltage at V_{REF} will still contain some noise and glitches from the SAR conversion process. These can be reduced by carefully bypassing the V_{REF} pin to ground as outlined in the sections that follow.

INTERNAL REFERENCE

The ADS7818 contains an on-board 2.5V reference, resulting in a 0V to 5V input range on the analog input. The specification table gives the various specifications for the

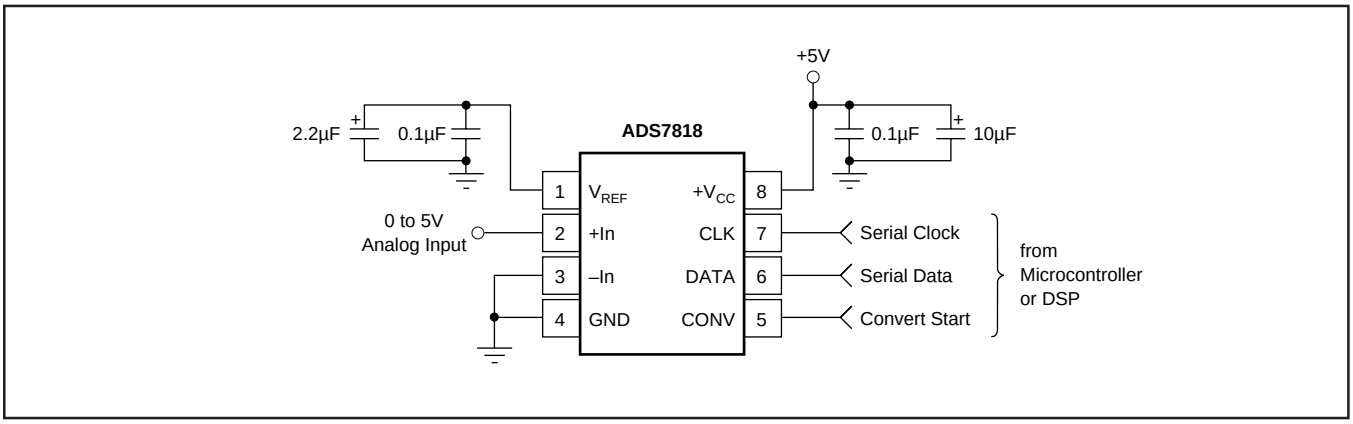


FIGURE 1. Basic Operation of the ADS7818.

internal reference. This reference can be used to supply a small amount of source current to an external load, but the load should be static. Due to the internal 10kΩ resistor, a dynamic load will cause variations in the reference voltage, and will dramatically affect the conversion result. Note that even a static load will reduce the internal reference voltage seen at the buffer input. The amount of reduction depends on the load and the actual value of the internal "10kΩ" resistor. The value of this resistor can vary by ±30%.

The V_{REF} pin should be bypassed with a 0.1µF capacitor placed as close as possible to the ADS7818 package. In addition, a 2.2 µF tantalum capacitor should be used in parallel with the ceramic capacitor. Placement of this capacitor is not as critical.

EXTERNAL REFERENCE

The internal reference is connected to the V_{REF} pin and to the internal buffer via a 10kΩ series resistor. Thus, the reference voltage can easily be overdriven by an external reference voltage. The voltage range for the external voltage is 2.0V to 2.55V, corresponding to an analog input range of 4.0V to 5.1V.

While the external reference will not source significant current into the V_{REF} pin, it does have to drive the series 10kΩ resistor that is terminated into the 2.5V internal reference (the exact value of the resistor will vary up to ±30% from part to part). In addition, the V_{REF} pin should still be bypassed to ground with at least a 0.1 µF ceramic capacitor (placed as close to the ADS7818 as possible). The reference will have to be stable with this capacitive load. Depending on the particular reference and A/D conversion speed, additional bypass capacitance may be required, such as the 2.2µF tantalum capacitor shown in Figure 1.

Reasons for choosing an external reference over the internal reference vary, but there are two main reasons. One is to achieve a given input range. For example, a 2.048V reference provides for a 0V to 4.095V input range—or 1mV per LSB. The other is to provide greater stability over temperature. The internal reference is typically 20ppm/°C which translates into a full-scale drift of roughly 1 output code for every 12°C (this does not take into account other sources of full-scale drift). If greater stability over temperature is needed, then an external reference with lower temperature drift will be required.

DIGITAL INTERFACE

Figure 2 shows the serial data timing and Figure 3 shows the basic conversion timing for the ADS7818. The specific timing numbers are listed in Table I. There are several important items in Figure 3 which give the converter additional capabilities over typical 8-pin converters. First, the transition from sample mode to hold mode is synchronous to the falling edge of CONV and is not dependent on CLK. Second, the CLK input is not required to be continuous during the sample mode. After the conversion is complete, the CLK may be kept LOW or HIGH.

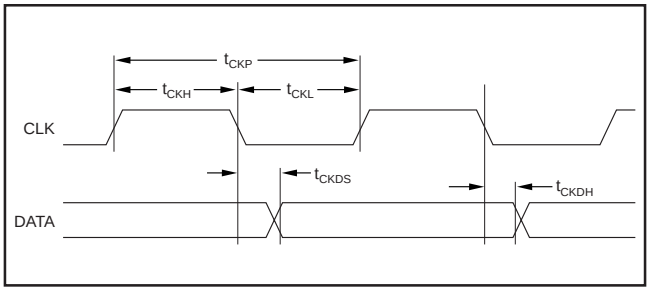


FIGURE 2. Serial Data and Clock Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	350			ns
t_{CONV}	Conversion Time	1.5			µs
t_{CKP}	Clock Period	125		5000	ns
t_{CKL}	Clock LOW	50			ns
t_{CKH}	Clock HIGH	50			ns
t_{CKDH}	Clock Falling to Current Data Bit No Longer Valid	5	15		ns
t_{CKDS}	Clock Falling to Next Data Valid		30	50	ns
t_{CVL}	CONV LOW	40			ns
t_{CVH}	CONV HIGH	40			ns
t_{CKCH}	CONV Hold after Clock Falls(1)	10			ns
t_{CKCS}	CONV Setup to Clock Falling(1)	10			ns
t_{CKDE}	Clock Falling to DATA Enabled		20	50	ns
t_{CKDD}	Clock Falling to DATA High Impedance		70	100	ns
t_{CKSP}	Clock Falling to Sample Mode		5		ns
t_{CKPD}	Clock Falling to Power-down Mode		50		ns
t_{CVHD}	CONV Falling to Hold Mode (Aperture Delay)		5		ns
t_{CVSP}	CONV Rising to Sample Mode		5		ns
t_{CVPU}	CONV Rising to Full Power-up		50		ns
t_{CVDD}	CONV Changing State to DATA High Impedance		70	100	ns
t_{CVPD}	CONV Changing State to Power-down Mode		50		ns
t_{DRP}	CONV Falling to Start of CLK (for hold droop < 0.1 LSB)			5	µs

Note: (1) This timing is not required under some situations. See text for more information.

TABLE I. Timing Specifications (T_A = –40°C to +85°C, C_{LOAD} = 30pF).

The asynchronous nature of CONV to CLK raises some interesting possibilities, but also some design considerations. Figure 3 shows that CONV has timing restraints in relation to CLK (t_{CKCH} and t_{CKCS}). However, if these times are violated (which could happen if CONV is completely asynchronous to CLK), the converter will perform a conversion correctly, but the exact timing of the conversion is indeterminate. Since the setup and hold time between CONV and CLK has been violated in this example, the start of conversion could vary by one clock cycle. (Note that the start of conversion can be detected by using a pull-up resistor on DATA. When DATA drops out of high-impedance and goes LOW, the conversion has started and that clock cycle is this first of the conversion.)

In addition if CONV is completely asynchronous to CLK and CLK is continuous, then there is possibility that CLK will transition just prior to CONV going LOW. If this occurs

faster than the 10ns indicated by t_{CKCH}, then there is a chance that some digital feedthrough may be coupled onto the hold capacitor. This could cause a small offset error for that particular conversion.

Thus, there are two basic ways to operate the ADS7818. CONV can be synchronous to CLK and CLK can be continuous. This would be the typical situation when interfacing the converter to a digital signal processor. The second method involves having CONV asynchronous to CLK and gating the operation of CLK (a non-continuous clock). This method would be more typical of an SPI-like interface on a microcontroller. This method would also allow CONV to be generated by a trigger circuit and to initiate (after some delay) the start of CLK. These two methods are covered under DSP Interfacing and SPI Interfacing.

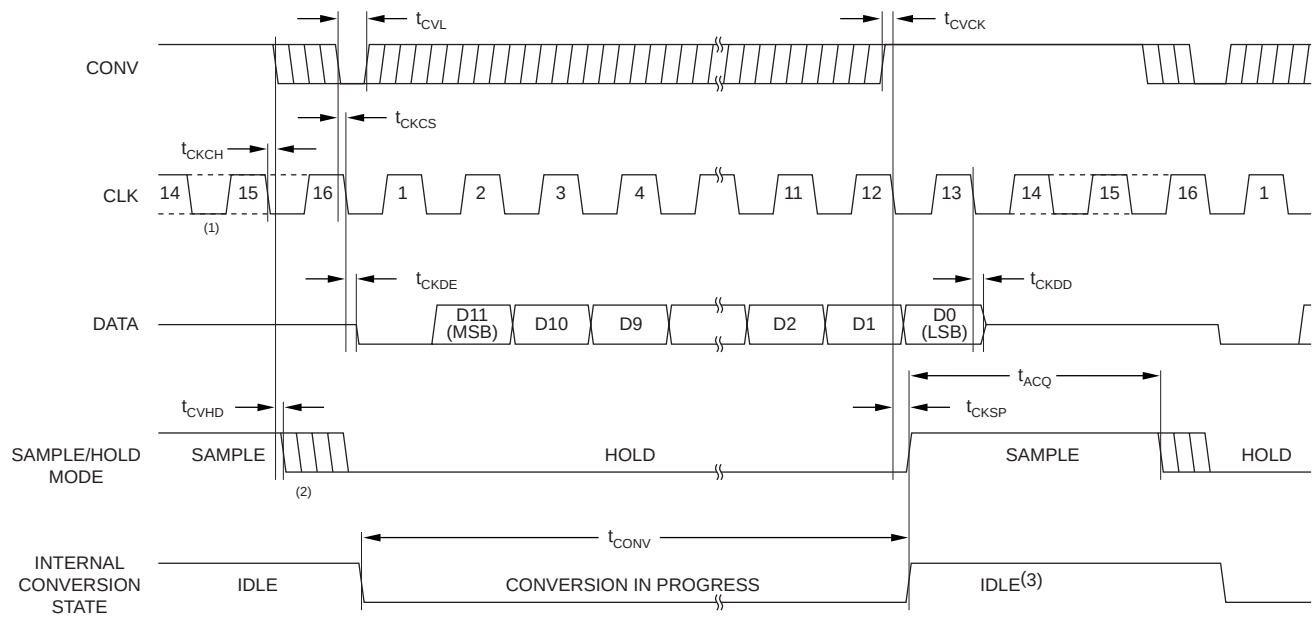
POWER-DOWN TIMING

The conversion timing shown in Figure 3 does not result in the ADS7818 going into the power-down mode. If the conversion rate of the device is high (approaching 500kHz), then there is very little power that can be saved by using the power-down mode. However, since the power-down mode incurs no conversion penalty (the very first conversion is valid), at lower sample rates, significant power can be saved by allowing the device to go into power-down mode between conversions.

Figure 4 shows the typical method for placing the A/D into the power-down mode. If CONV is kept LOW during the conversion and is LOW at the start of the 13 clock cycle, then the device enters the power-down mode. It remains in this mode until the rising edge of CONV. Note that CONV must be HIGH for at least t_{ACQ} in order to sample the signal properly as well as to power-up the internal nodes.

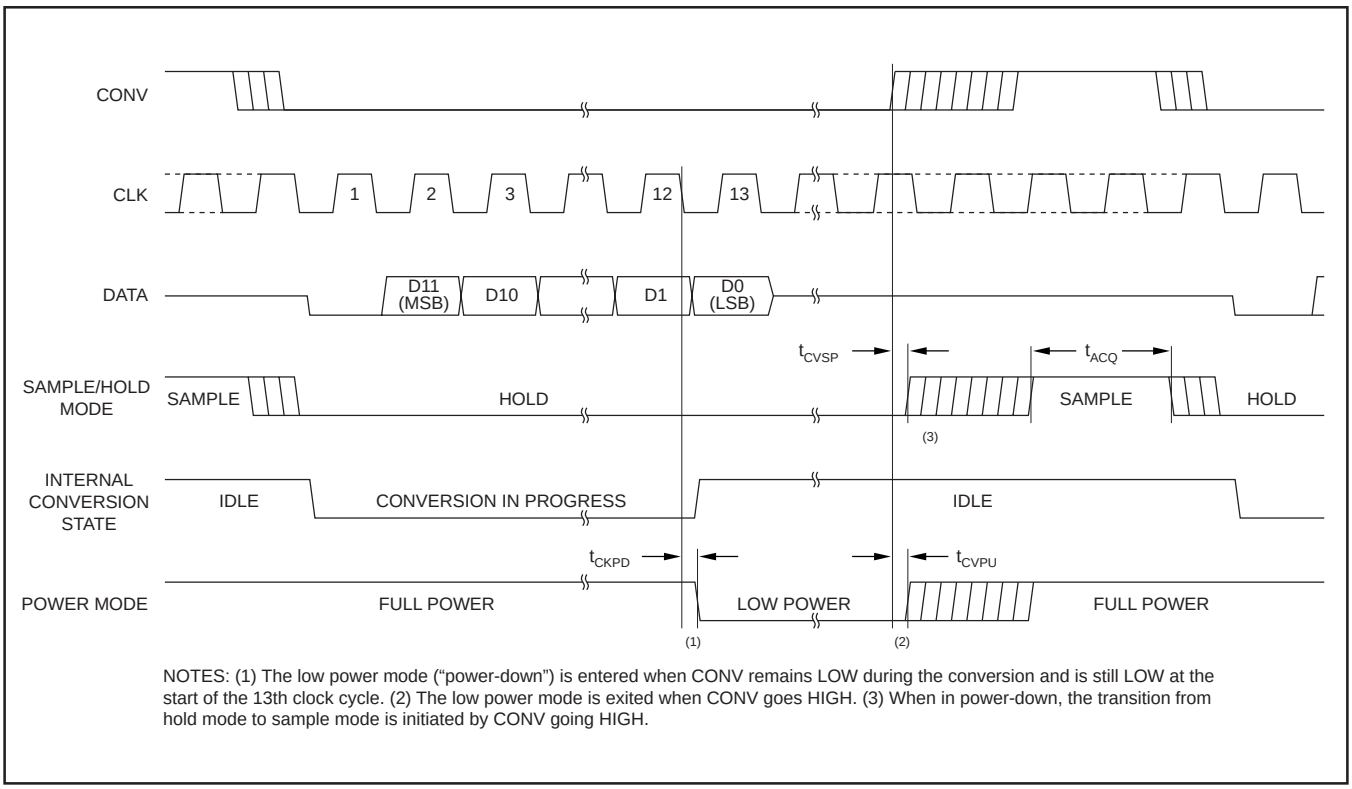
There are two different methods for clocking the ADS7818. The first involves scaling the CLK input in relation to the conversion rate. For example, an 8MHz input clock and the timing shown in Figure 3 results in a 500kHz conversion rate. Likewise, a 1.6MHz clock would result in a 100kHz conversion rate. The second method involves keeping the clock input as close to the maximum clock rate as possible and starting conversions as needed. This timing is similar to that shown in Figure 4. As an example, a 50kHz conversion rate would require 160 clock periods per conversion instead of the 16 clock periods used at 500kHz.

The main distinction between the two is the amount of time that the ADS7818 remains in power down. In the first mode, the converter only remains in power down for a small number of clock periods (depending on how many clock periods there are per each conversion). As the conversion rate scales, the converter always spends the same percentage of time in power down. Since less power is drawn by the digital logic, there is a small decrease in power consumption, but it is very slight. This effect can be seen in the typical performance curve “Supply Current vs Sample Rate.”



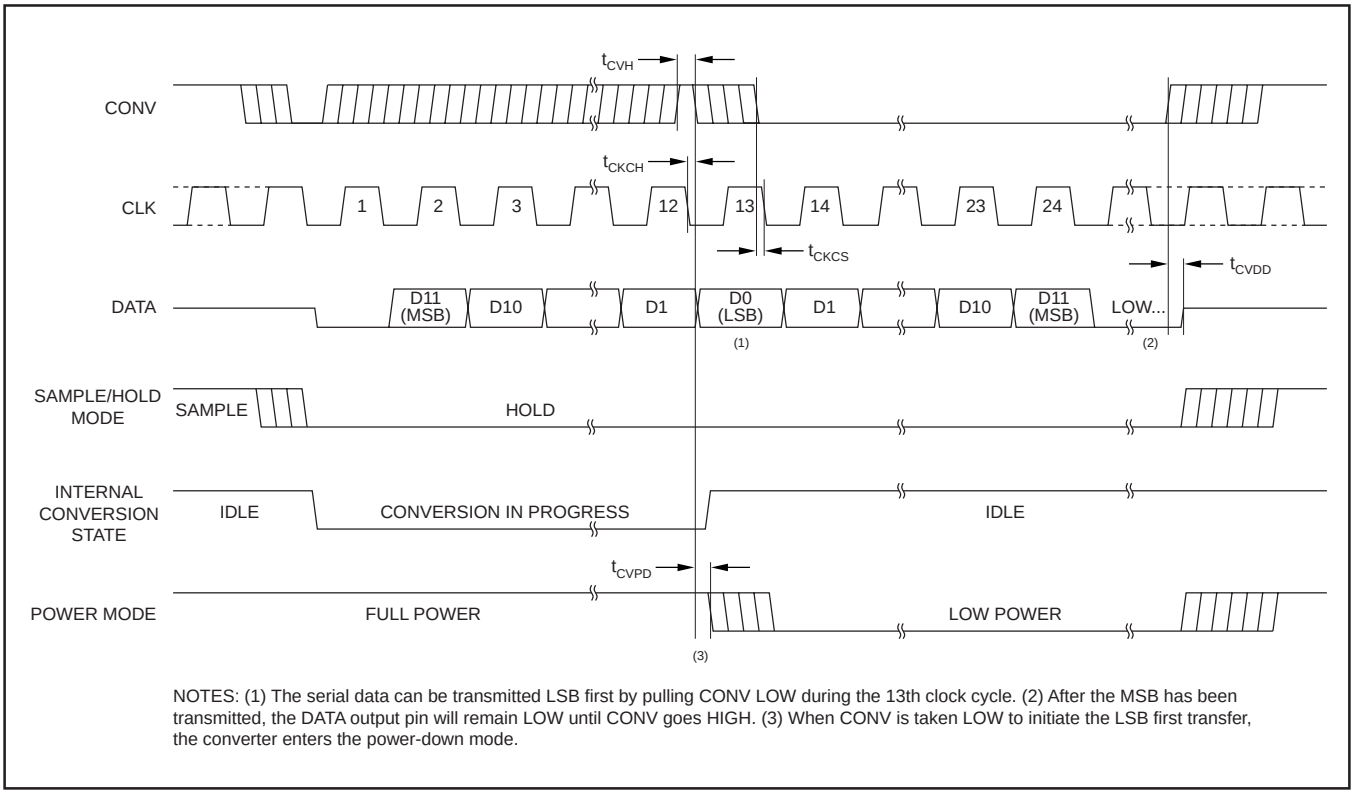
NOTES: (1) Clock periods 14 and 15 are shown for clarity, but are not required for proper operation of the ADS7818, provided that the minimum t_{ACQ} time is met. The CLK input may remain HIGH or LOW during this period. (2) The transition from sample mode to hold mode occurs on the falling edge of CONV. This transition is not dependent on CLK. (3) The device remains fully powered when operated as shown. If the sample time is longer than 3 clock periods, power consumption can be reduced by allowing the device to enter a power down mode. See the power down timing for more information.

FIGURE 3. Basic Conversion Timing.



NOTES: (1) The low power mode ("power-down") is entered when CONV remains LOW during the conversion and is still LOW at the start of the 13th clock cycle. (2) The low power mode is exited when CONV goes HIGH. (3) When in power-down, the transition from hold mode to sample mode is initiated by CONV going HIGH.

FIGURE 4. Power-down Timing.



NOTES: (1) The serial data can be transmitted LSB first by pulling CONV LOW during the 13th clock cycle. (2) After the MSB has been transmitted, the DATA output pin will remain LOW until CONV goes HIGH. (3) When CONV is taken LOW to initiate the LSB first transfer, the converter enters the power-down mode.

FIGURE 5. Serial Data "LSB-First" Timing.

In contrast, the second method (clocking at a fixed rate) means that each conversion takes X clock cycles. As the time between conversions get longer, the converter remains in power-down an increasing percentage of time. This reduces total power consumption by a considerable amount. For example, a 50kHz conversion rate results in roughly 1/10 of the power (minus the reference) that is used at a 500kHz conversion rate.

Table II offers a look at the two different modes of operation and the difference in power consumption.

f_{SAMPLE}	POWER WITH CLK = 16 • f_{SAMPLE}	POWER WITH CLK = 8MHz
500kHz	11mW	11mW
250kHz	10mW	7mW
100kHz	9mW	4mW

TABLE II. Power Consumption versus CLK Input.

LSB FIRST DATA TIMING

Figure 5 shows a method to transmit the digital result in a least-significant bit (LSB) format. This mode is entered when CONV is pulled HIGH during the conversion (before the end of the 12th clock) and then pulled LOW during the 13th clock (when D0, the LSB, is being transmitted). The next 11 clocks then repeat the serial data, but in an LSB first format. The converter enters the power-down mode during the 13th clock and resumes normal operation when CONV goes HIGH.

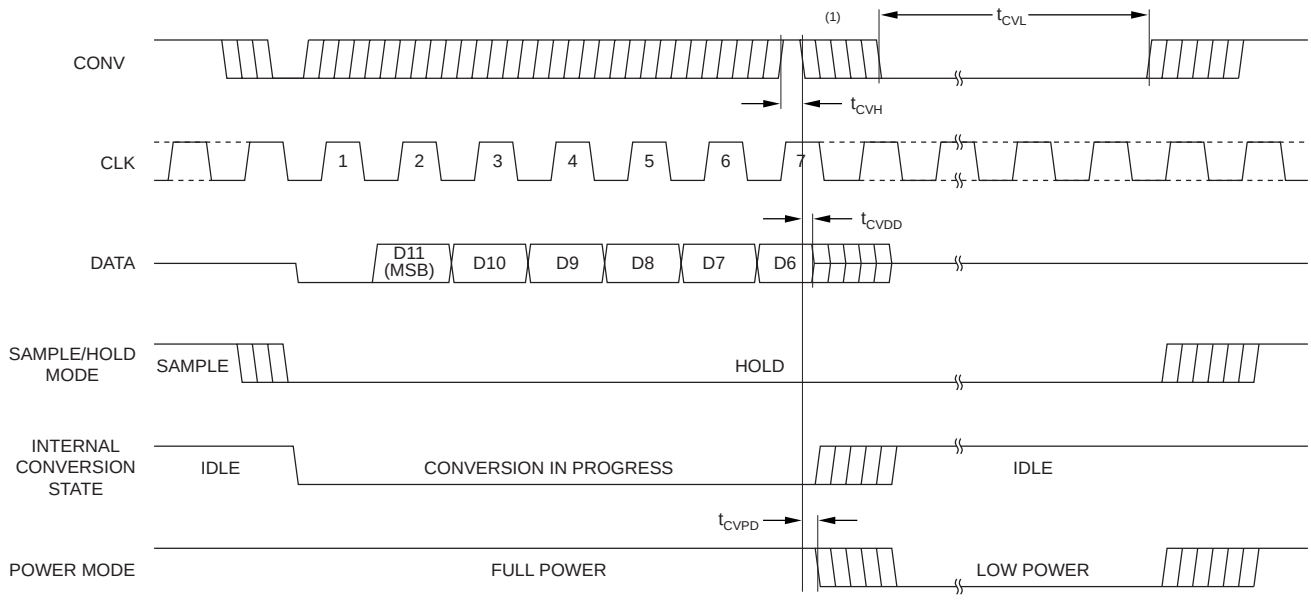
SHORT-CYCLE TIMING

The conversion currently in progress can be "short-cycled" with the technique shown in Figure 6. This term means that the conversion will terminate immediately, before all 12-bits have been decided. This can be a very useful feature when a resolution of 12-bits is not needed. An example would be when the converter is being used to monitor an input voltage until some condition is met. At that time, the full resolution of the converter would then be used. Short-cycling the conversion can result in a faster conversion rate or lower power dissipation.

There are several very important items shown in Figure 6. The conversion currently in progress is terminated when CONV is taken HIGH during the conversion and then taken LOW prior to t_{CKCH} before the start of the 13th clock cycle. Note that if CONV goes LOW during the 13th clock cycle, then the LSB first mode will be entered (Figure 5). Also, when CONV goes LOW, the DATA output immediately transitions to high impedance. If the output bit that is present during that clock period is needed, CONV must not go LOW until the bit has been properly latched into the receiving logic.

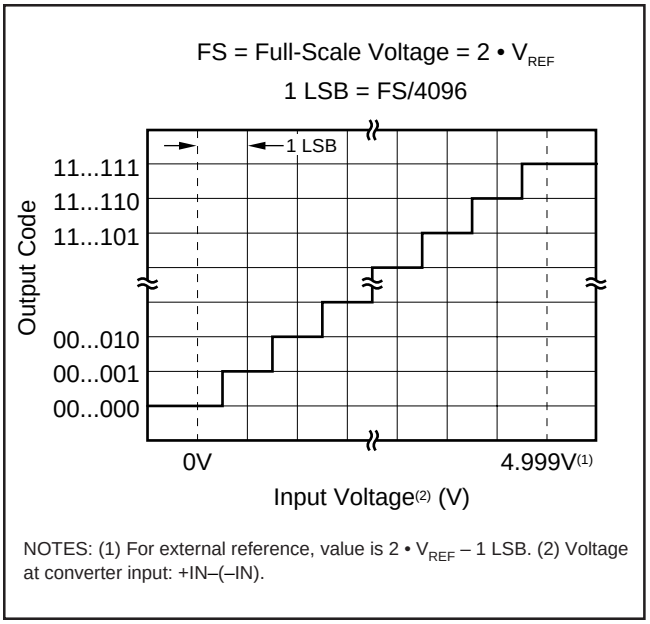
DATA FORMAT

The ADS7818 output data is in straight binary format as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTE: (1) The conversion currently in progress can be stopped by pulling CONV LOW during the conversion. This must occur at least t_{CKCS} prior to the start of the 13th clock cycle. The DATA output pin will tri-state and the device will enter the power-down mode when CONV is pulled LOW.

FIGURE 6. Short-cycle Timing.



NOTES: (1) For external reference, value is 2 • V_{REF} – 1 LSB. (2) Voltage at converter input: +IN–(–IN).

FIGURE 7. Ideal Input Voltages and Output Codes.

DSP INTERFACING

Figure 8 shows a timing diagram that might be used with a typical digital signal processor such as a TI DSP. For the buffered serial port (BSP) on the TMS320C54X family, CONV would tied to BFSX, CLK would be tied to BCLKX, and DATA would be tied to BDR.

SPI/QSPI INTERFACING

Figure 9 shows the timing diagram for a typical serial peripheral interface (SPI) or queued serial peripheral interface (QSPI). Such interfaces are found on a number of microcontrollers form various manufacturers. CONV would be tied to a general purpose I/O pin (SPI) or to a PCX pin (QSPI), CLK would be tied to the serial clock, and DATA would be tied to the serial input data pin such as MISO (master in slave out).

Note the time t_{DRP} shown in Figure 9. This represents the maximum amount of time between CONV going LOW and the start of the conversion clock. Since CONV going LOW places the sample and hold in the hold mode and because the hold capacitor looses charge over time, there is a requirement that time t_{DRP} be met as well as the maximum clock period (t_{CKP}).

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7818 circuitry. This is particularly true if the CLK input is approaching the maximum input rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the CLK input.

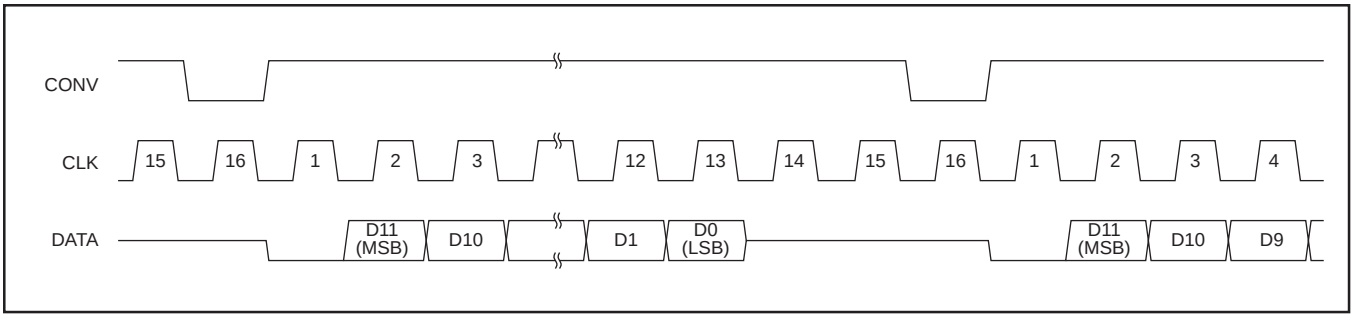


FIGURE 8. Typical DSP Interface Timing.

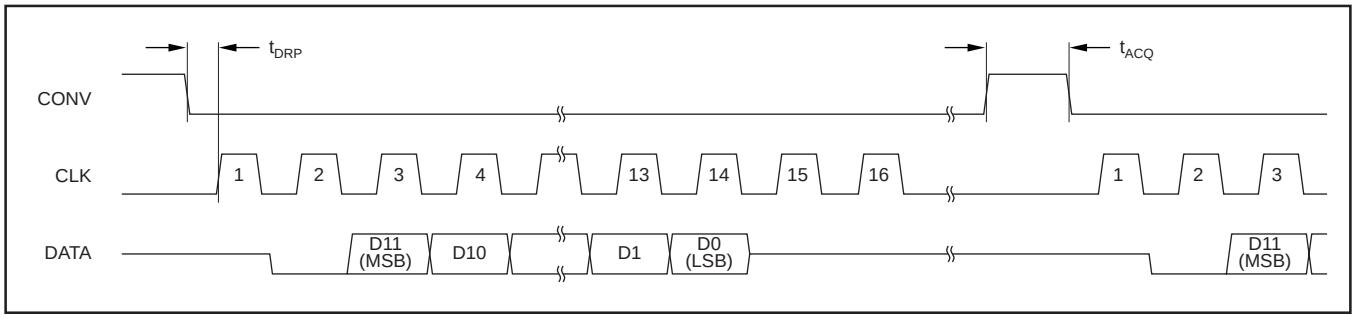


FIGURE 9. Typical SPI/QSPI Interface Timing.

With this in mind, power to the ADS7818 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor my be used to lowpass filter a noisy supply.

The ADS7818 draws very little current from an external reference on average as the reference voltage is internally buffered. However, glitches from the conversion process appear at the V_{REF} input and the reference source must be able to handle this. Whether the reference is internal or external, the V_{REF} pin should be bypassed with a 0.1µF capacitor. An additional larger capacitor may also be used, if desired. If the reference voltage is external and originates from an op-amp, make sure that it can drive the bypass capacitor or capacitors without oscillation.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS7818E/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818E/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818E/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818E/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818EB/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818EB/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818EB/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818EB/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7818P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7818PB	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7818PBG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7818PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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SBAS035B – FEBRUARY 1995 – REVISED FEBRUARY 2005

12-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW POWER: 390mW
- INTERNAL REFERENCE
- WIDEBAND TRACK-AND-HOLD: 65MHz
- SINGLE +5V SUPPLY

APPLICATIONS

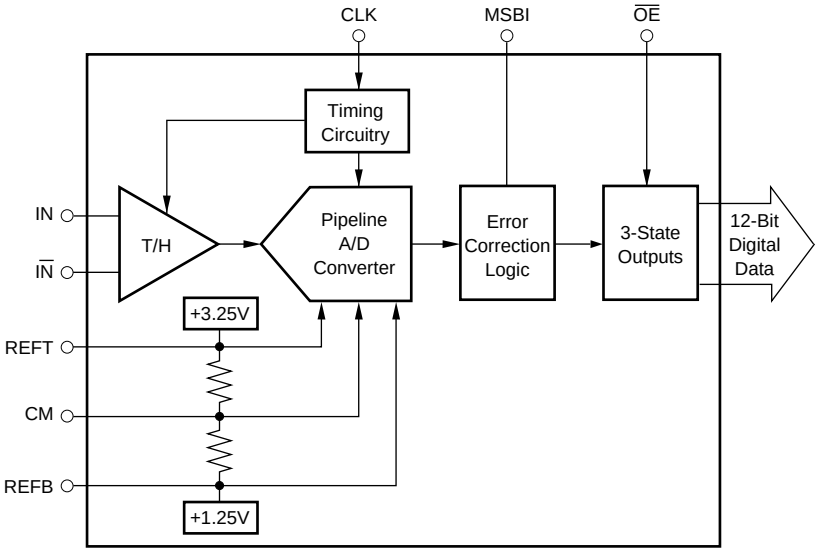
- IF AND BASEBAND DIGITIZATION
- DIGITAL COMMUNICATIONS
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING

DESCRIPTION

The ADS800 is a low-power, monolithic 12-bit, 40MHz Analog-to-Digital (A/D) converter utilizing a small geometry CMOS process. This complete converter includes a 12-bit quantizer, wideband track-and-hold, reference, and three-state outputs. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS800 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR, and high oversampling capability give it the extra margin needed for telecommunications, test instrumentation, and video applications.

This high-performance A/D converter is specified over temperature for AC and DC performance at a 40MHz sampling rate. The ADS800 is available in an SO-28 package.



ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V Max
External Bottom Reference Voltage (REFB)	+1.1V Min

NOTE: (1) Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS800U	SO-28	DW	–40°C to +85°C	ADS800U	ADS800U	Rails, 28

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

			ADS800U			
PARAMETER	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Resolution				12		Bits
Specified Temperature Range	$T_{AMBIENT}$		0		+70	°C
Operating Temperature Range	$T_{AMBIENT}$		–40		+85	°C
ANALOG INPUT						
Differential Full-Scale Input Range	Both Inputs, 180° Out-of-Phase		+1.25		+3.25	V
Common-Mode Voltage				+2.25		V
Analog Input Bandwidth (–3dB)						
Small-Signal	–20dBFS[1] Input	+25°C		400		MHz
Full-Power	0dBFS Input	+25°C		65		MHz
Input Impedance				1.25 || 4		MΩ || pF
DIGITAL INPUT						
Logic Family				TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge		
ACCURACY[2]		f_S = 2.5MHz				
Gain Error		+25°C		±0.4	±1.5	%
		Full		±0.6	±2.5	%
Gain Drift				±95		ppm/°C
Power-Supply Rejection of Gain	$\Delta +V_S$ = ±5%	+25°C		0.01	0.15	%FSR/%
Input Offset Error		Full		±2.6	±3.5	%
Power-Supply Rejection of Offset	$\Delta +V_S$ = ±5%	+25°C		0.02	0.15	%FSR/%
CONVERSION CHARACTERISTICS						
Sample Rate			10k		40M	Sample/s
Data Latency				6.5		Convert Cycle
DYNAMIC CHARACTERISTICS						
Differential Linearity Error						
f = 500kHz	t_H = 13ns[3]	+25°C		±0.6	±1.0	LSB
		Full		±0.8		LSB
f = 12MHz		+25°C		±0.4	±1.0	LSB
		Full		±0.5		LSB
No Missing Codes	t_H = 13ns[3]	+25°C		Tested		LSB
Integral Linearity Error at f = 500kHz		Full		±1.9		LSB
Spurious-Free Dynamic Range (SFDR)						
f = 500kHz (–1dBFS input)		+25°C	65	72		dBFS
		Full	60	66		dBFS
f = 12MHz (–1dBFS input)		+25°C	58	61		dBFS
		Full	55	61		dBFS

NOTES: (1) dBFS refers to dB below Full-Scale. (2) Percentage accuracies are referred to the internal A/D converter Full-Scale Range of 4Vp-p. (3) To assure DNL and no missing code performance, see timing diagram footnote 2. (4) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (5) No "rollover" of bits.

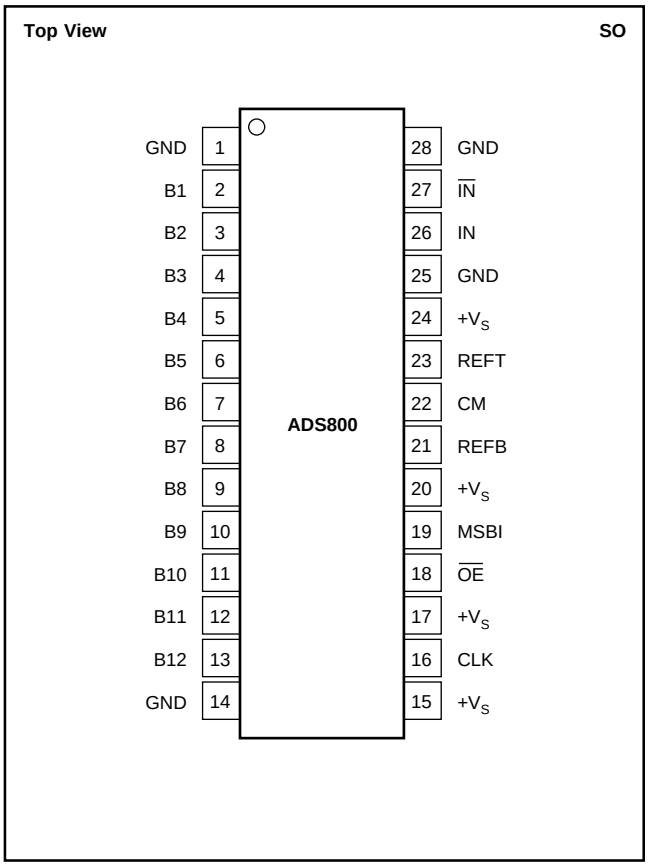
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS800U MIN	ADS800U TYP	ADS800U MAX	UNITS
DYNAMIC CHARACTERISTICS (Cont.)						
2-Tone Intermodulation Distortion (IMD)[4]						
f = 4.4MHz and 4.5MHz (–7dBFS each tone)		+25°C		–63		dBc
		Full		–62		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dBFS input)		+25°C	61	64		dB
		Full	57	63		dB
f = 12MHz (–1dBFS input)		+25°C	61	62		dB
		Full	56	62		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		+25°C	59	63		dB
		Full	54	64		dB
f = 12MHz (–1dBFS input)		+25°C	56	58		dB
		Full	51	57		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5		%
Differential Phase Error	NTSC or PAL	+25°C		0.1		degrees
Aperture Delay Time		+25°C		2		ns
Aperture Jitter		+25°C		7		ps rms
Over-Voltage Recovery Time[5]	1.5x Full-Scale Input	+25°C		2		ns
OUTPUTS						
Logic Family				TTL/HCT Compatible CMOS		
Logic Coding		Logic Selectable		SOB or BTC		
Logic Levels	Logic “LO”, C_L = 15pF max	Full	0		0.4	V
	Logic “HI”, C_L = 15pF max	Full	+2.5		$+V_S$	V
3-State Enable Time				20	40	ns
3-State Disable Time		Full		2	10	ns
POWER-SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating	+25°C		78	93	mA
	Operating	Full		78	97	mA
Power Consumption	Operating	+25°C		390	465	mW
	Operating	Full		390	485	mW
Thermal Resistance, θ_{JA}						
SO-28				75		°C/W

NOTES: (1) dBFS refers to dB below Full-Scale. (2) Percentage accuracies are referred to the internal A/D converter Full-Scale Range of 4Vp-p. (3) To assure DNL and no missing code performance, see timing diagram footnote 2. (4) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (5) No “rollover” of bits.

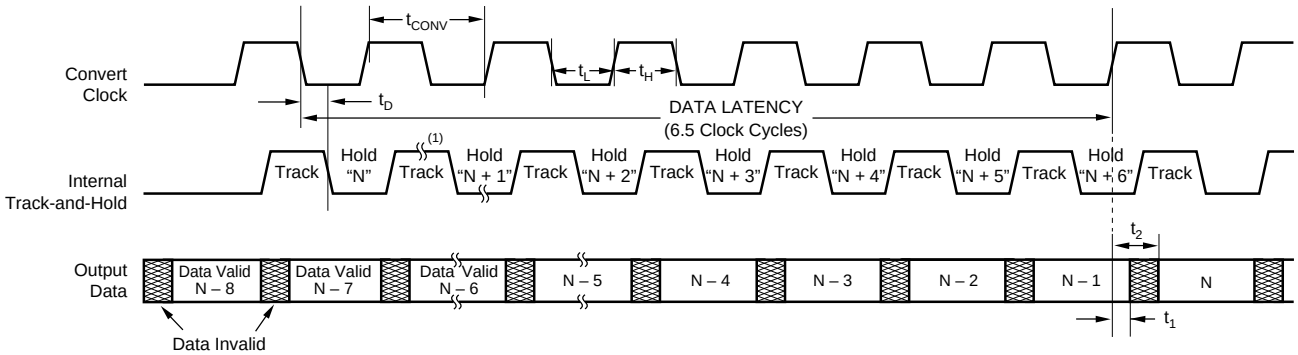
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10
12	B11	Bit 11
13	B12	Bit 12, Least Significant Bit
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	IN	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM



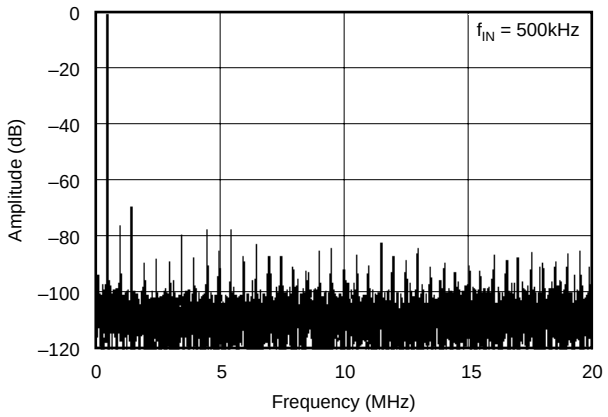
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		100µs	ns
t_L	Clock Pulse LOW	12	12.5		ns
t_H	Clock Pulse HIGH	12(2)	12.5		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

NOTES: (1) " ⟆ " indicates the portion of the waveform that will stretch out at slower sample rates. (2) t_H must be 13ns minimum if no missing codes is desired only for the conditions of $t_{CONV} \leq 28ns$ and $f_{IN} < 2MHz$.

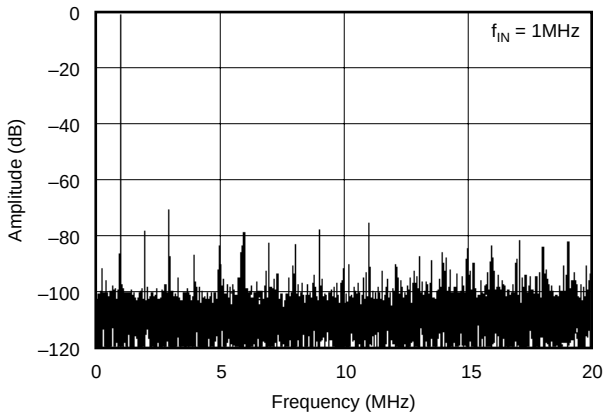
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

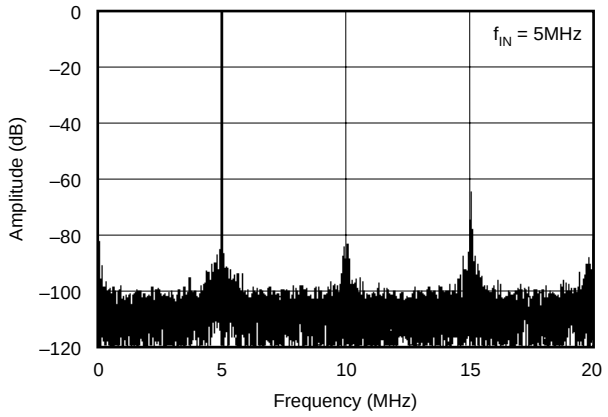
SPECTRAL PERFORMANCE



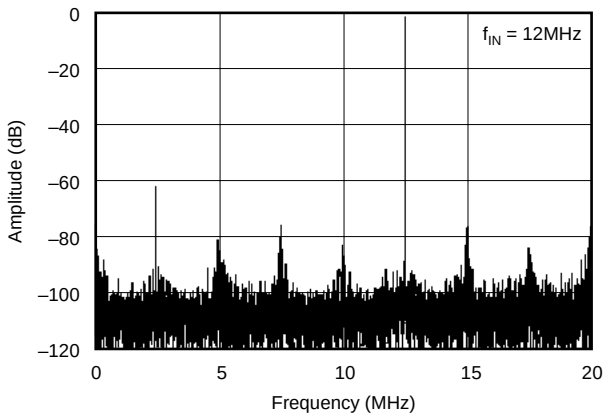
SPECTRAL PERFORMANCE



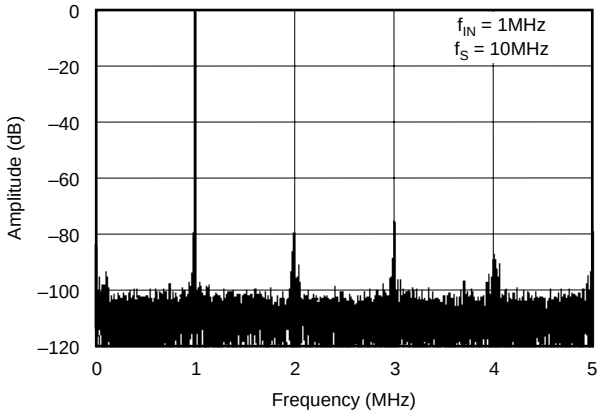
SPECTRAL PERFORMANCE



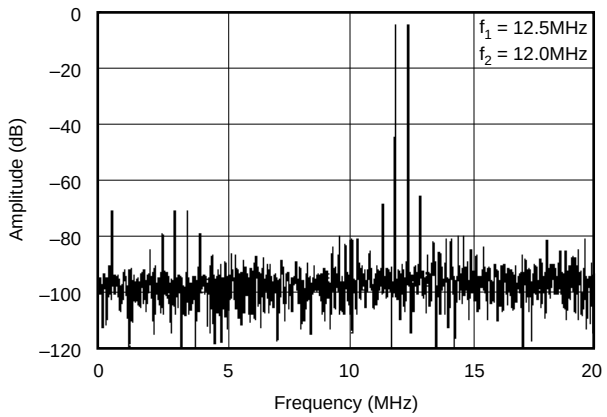
SPECTRAL PERFORMANCE



SPECTRAL PERFORMANCE



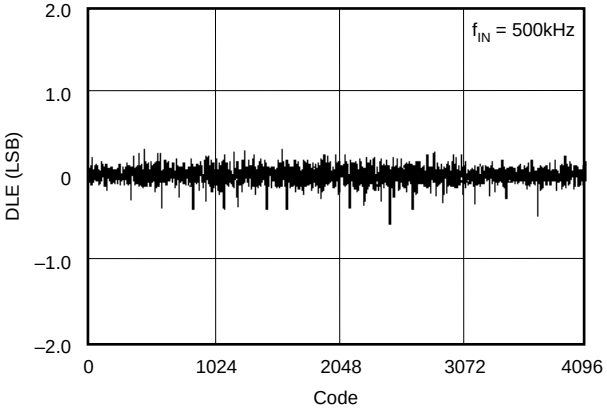
2-TONE INTERMODULATION



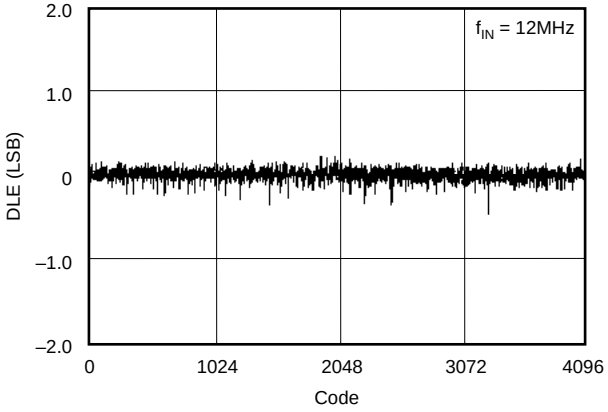
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

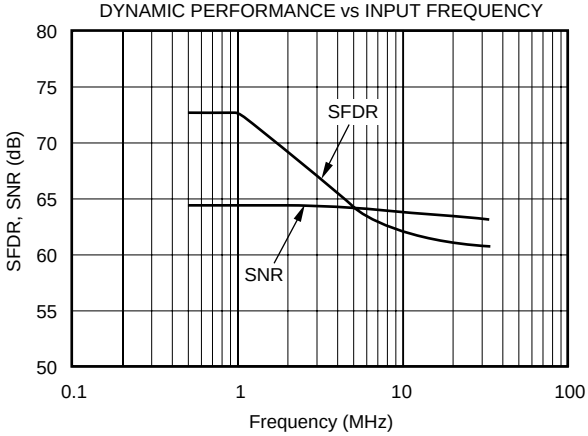
DIFFERENTIAL LINEARITY ERROR



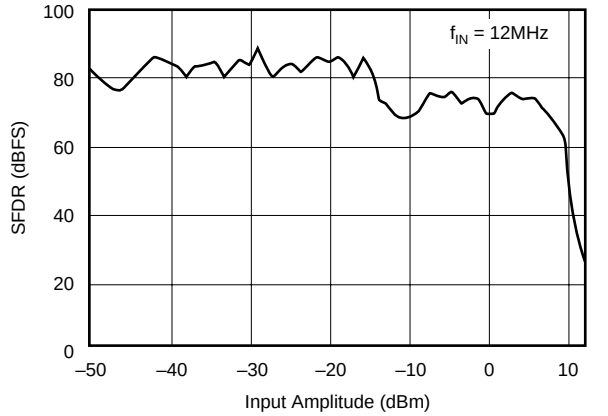
DIFFERENTIAL LINEARITY ERROR



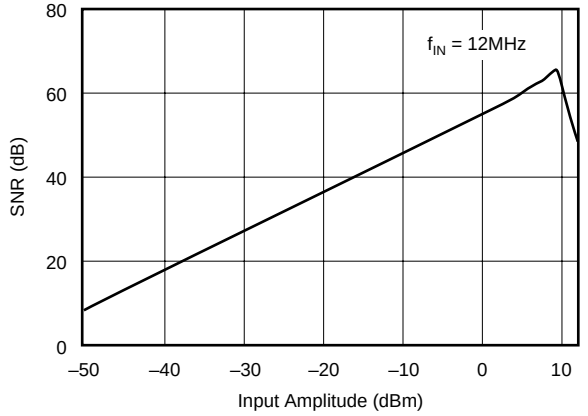
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



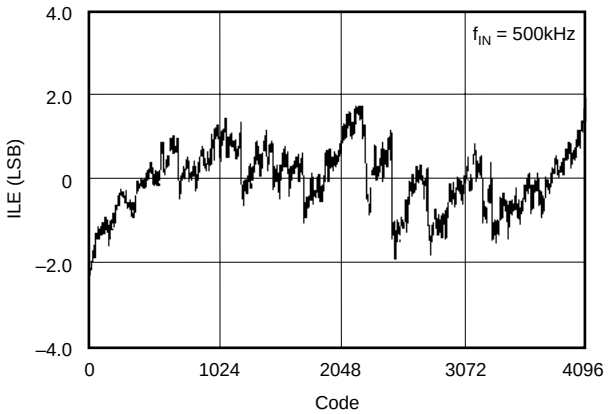
SWEPT POWER SFDR



SWEPT POWER SNR



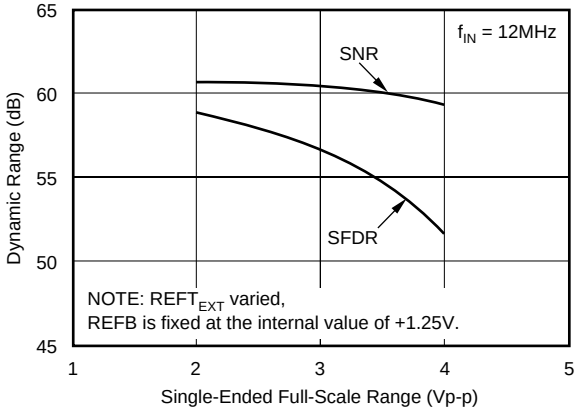
INTEGRAL LINEARITY ERROR



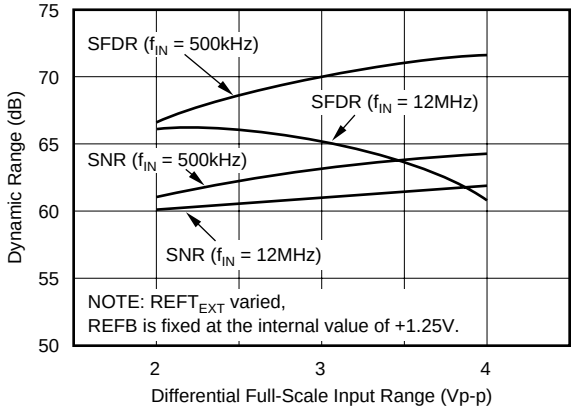
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

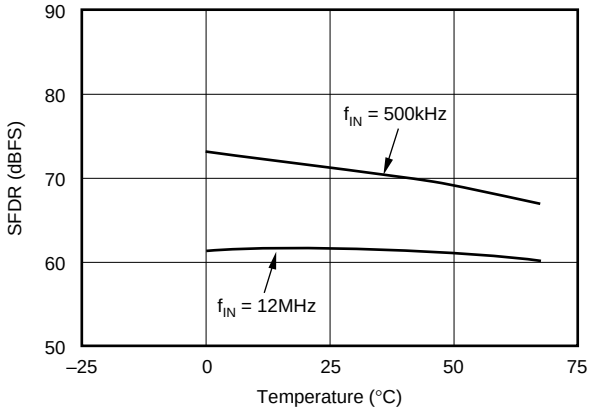
DYNAMIC PERFORMANCE
vs SINGLE-ENDED FULL-SCALE INPUT RANGE



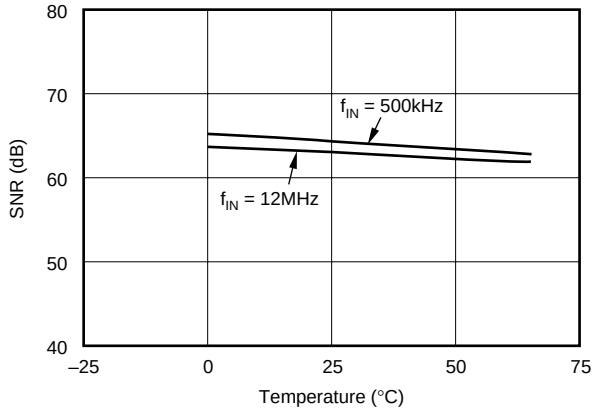
DYNAMIC PERFORMANCE
vs DIFFERENTIAL FULL-SCALE INPUT RANGE



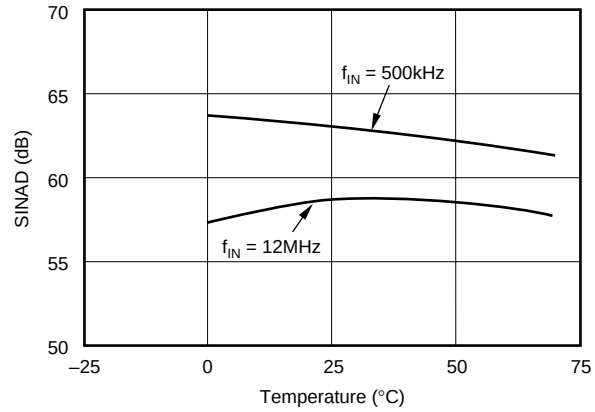
SPURIOUS-FREE DYNAMIC RANGE (SFDR)
vs TEMPERATURE



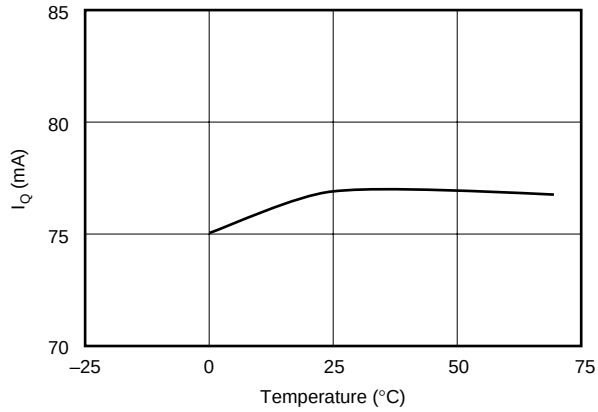
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



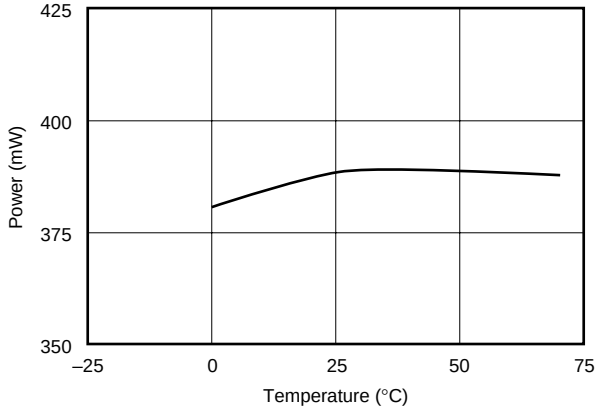
SUPPLY CURRENT vs TEMPERATURE



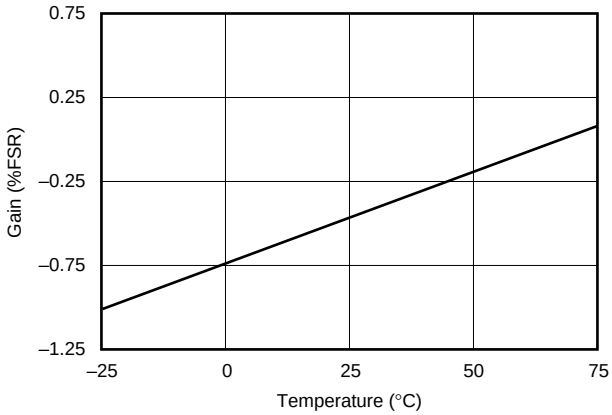
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

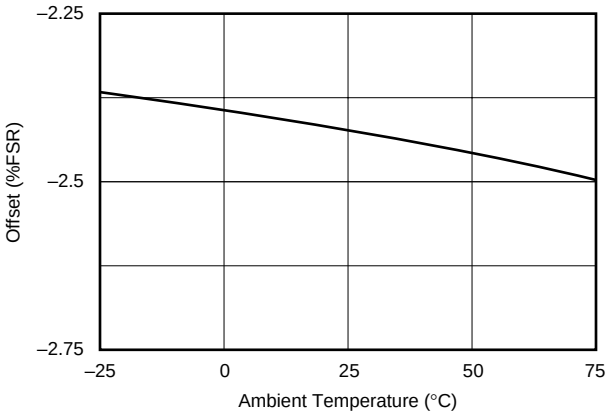
POWER DISSIPATION vs TEMPERATURE



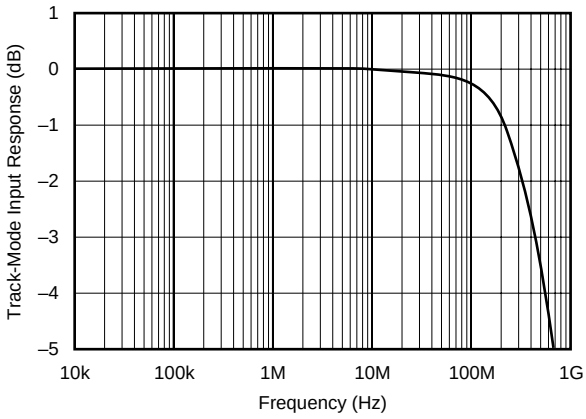
GAIN ERROR vs TEMPERATURE



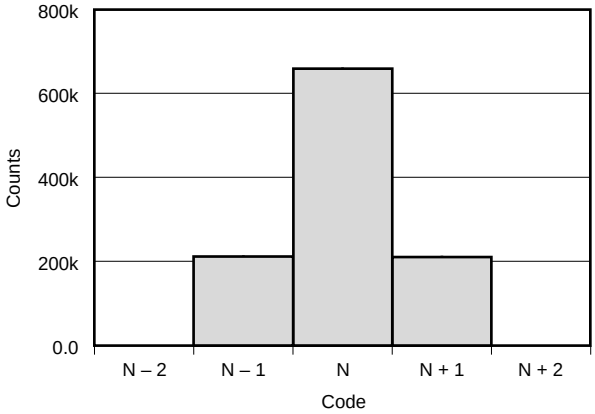
OFFSET ERROR vs TEMPERATURE



TRACK-MODE SMALL-SIGNAL INPUT BANDWIDTH



OUTPUT NOISE HISTOGRAM (NO SIGNAL)



THEORY OF OPERATION

The ADS800 is a high-speed, sampling A/D converter with pipelining. It uses a fully differential architecture and digital error correction to ensure 12-bit resolution. The differential track-and-hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping 2-phase signal, $\phi1$ and $\phi2$. At the sampling time, the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time, the charge redistributes between C_I and C_H, completing one track-and-hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track-and-hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 11 stages with each stage containing a 2-bit quantizer and a 2-bit Digital-to-Analog Converter (DAC), as shown in Figure 2. Each 2-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to time-

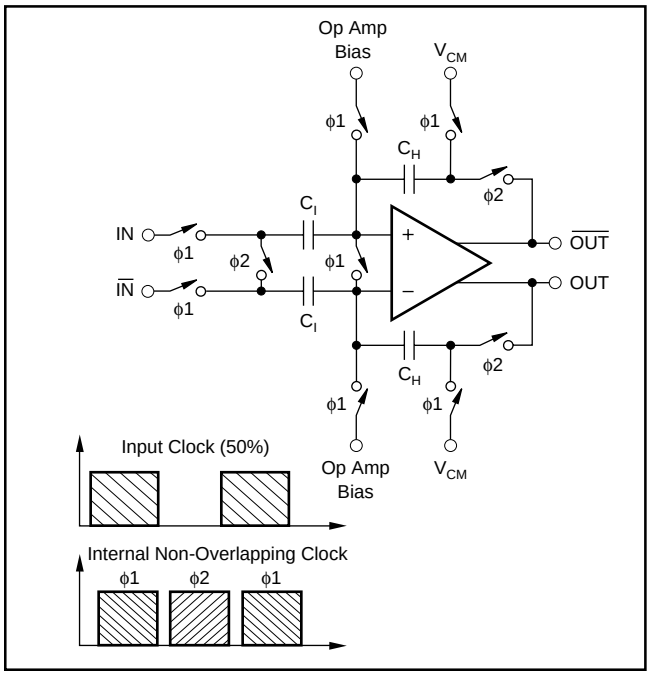


FIGURE 1. Input Track-and-Hold Configuration with Timing Signals.

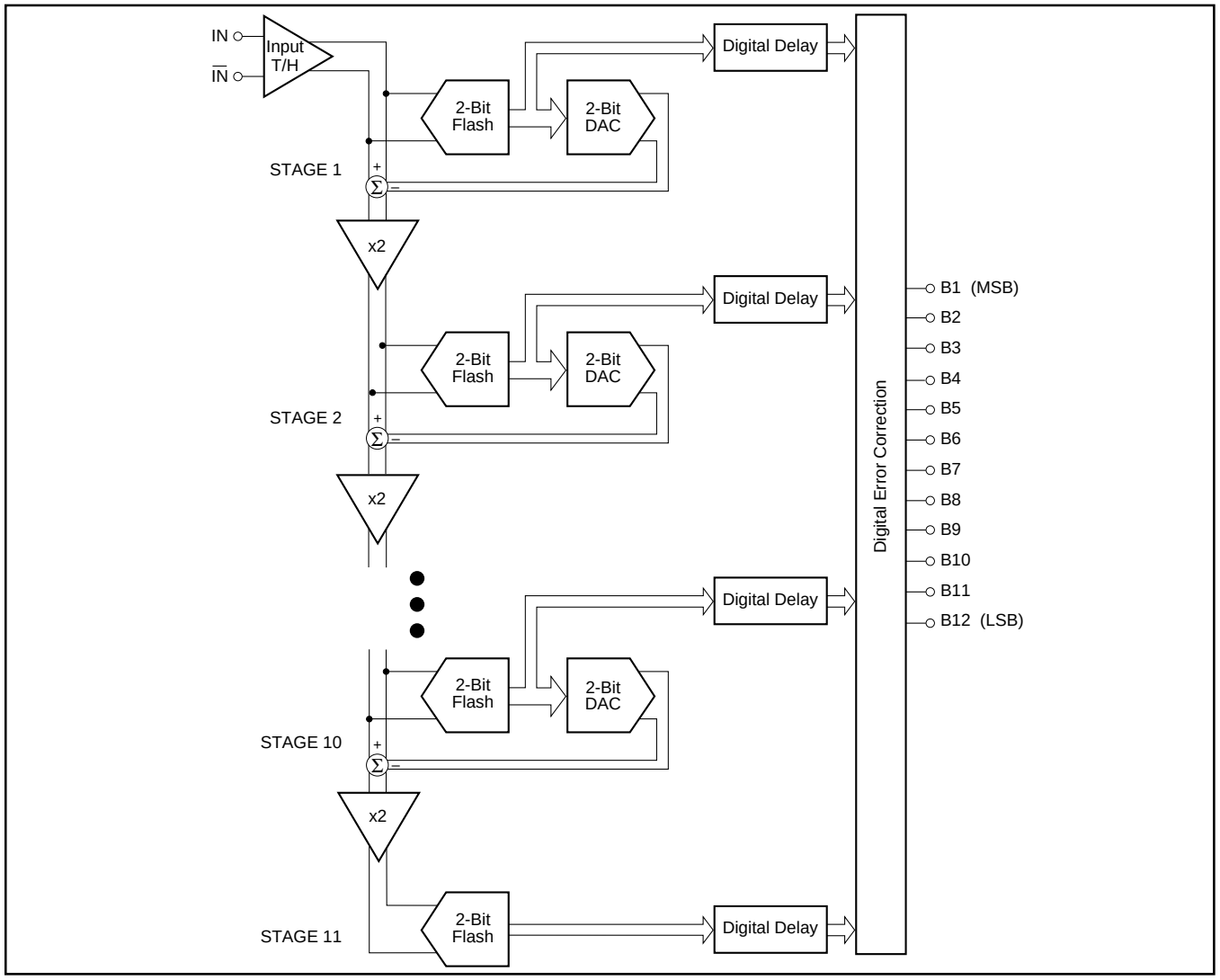


FIGURE 2. Pipeline A/D Converter Architecture.

align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS800 excellent differential linearity and ensures no missing codes at the 12-bit level.

Since there are two pipeline stages per external clock cycle, there is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS800 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS800 has an internal reference that sets the full-scale input range of the A/D converter. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full-scale range of +1.25V to +3.25V. Since each input is 2Vp-p and 180° out-of-phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full-scale reference (REFT) and the negative full-scale (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended input, and ADS800 drive circuits, refer to the applications section.

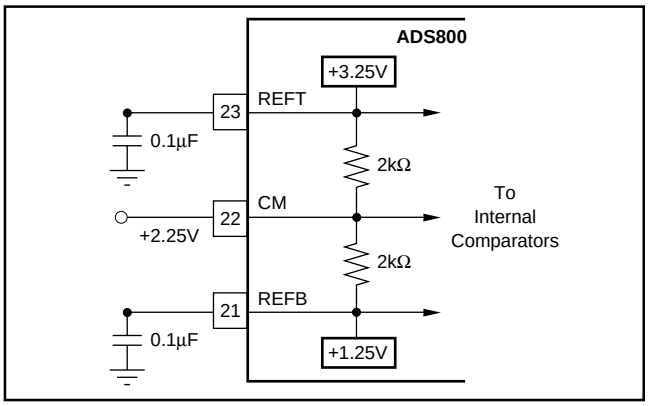


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. Both the rising and falling edges of the externally applied clock control the various interstage conversions in the pipeline. Therefore, the clock signal's jitter, rise-and-fall times, and duty cycle can affect conversion performance.

- Low clock **jitter** is critical to SNR performance in frequency-domain signal environments.
- Clock **rise-and-fall times** should be as short as possible (< 2ns for best performance).
- For most applications, the clock duty should be set to 50%. However, for applications requiring no missing codes, a slight skew in the duty cycle will improve DNL performance for conversion rates > 35MHz and input frequencies < 2MHz (see Timing Diagram) in the SO package. For the best performance in the SSOP package, the clock should be skewed under all input frequencies with conversion rates > 35MHz. A possible method for skewing the 50% duty cycle source is shown in Figure 4.

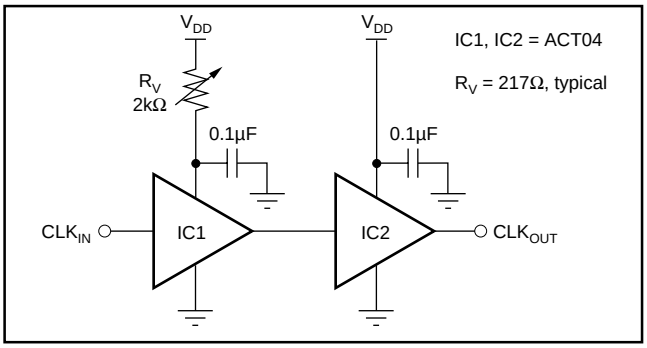


FIGURE 4. Clock Skew Circuit.

DIGITAL OUTPUT DATA

The 12-bit output data is provided at CMOS logic levels. The standard output coding is Straight Offset Binary (SOB) where a full-scale input signal corresponds to all "1's" at the output, as shown in Table 1. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a logic "HI" voltage to this pin, a Binary Two's Complement (BTC) output will be provided where the most significant bit is inverted. The digital outputs of the ADS800 can be set to a high-impedance state by driving $\overline{OE}$ (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

	OUTPUT CODE	
DIFFERENTIAL INPUT[1]	SOB PIN 19 FLOATING or LO	BTC PIN 19 HI
+FS (IN = +3.25V, $\overline{IN}$ = +1.25V)	111111111111	011111111111
+FS – 1LSB	111111111111	011111111111
+FS – 2LSB	111111111110	011111111110
+3/4 Full-Scale	111000000000	011000000000
+1/2 Full-Scale	110000000000	010000000000
+1/4 Full-Scale	101000000000	001000000000
+1LSB	100000000001	000000000001
Bipolar Zero (IN = $\overline{IN}$ = +2.25V)	100000000000	000000000000
–1LSB	011111111111	111111111111
–1/4 Full-Scale	011000000000	111000000000
–1/2 Full-Scale	010000000000	110000000000
–3/4 Full-Scale	001000000000	101000000000
–FS + 1LSB	000000000001	100000000001
–FS (IN = +1.25V, $\overline{IN}$ = +3.25V)	000000000000	100000000000

NOTE: (1) In the single-ended input mode, +FS = +4.25V and –FS = +0.25V.

TABLE I. Coding Table for the ADS800.

APPLICATIONS

DRIVING THE ADS800

The ADS800 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential output is created on the secondary if the center tap is tied to the common-mode voltage of +2.25V, as per Figure 5. This transformer-coupled input arrangement provides good high-frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full-scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the Common-Mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{IN}$ inputs should be bypassed with 22pF capacitors to minimize track-and-hold glitches and to improve high input frequency performance.

Figure 6 illustrates another possible low-cost interface circuit which utilizes resistors and capacitors in place of a transformer. Depending on the signal bandwidth, the component values should be carefully selected in order to maintain the product performance. The input capacitors, C_{IN}, and the input resistors, R_{IN}, create a high-pass filter with the lower corner frequency at $f_C = 1/(2pR_{IN}C_{IN})$. The corner frequency can be reduced by either increasing the value of R_{IN} or C_{IN}. If the circuit operates with a 50Ω or 75Ω impedance level, the resistors are fixed and only the value of the capacitor can be increased. Usually, AC-coupling capacitors are electrolytic or tantalum capacitors with values of 1µF or higher. It should be noted that these large capacitors become inductive with increased input frequency, which could lead to signal amplitude errors or oscillation. To maintain a low AC-coupling impedance throughout the signal band, a small value (e.g. 1µF) ceramic capacitor could be added in parallel with the polarized capacitor.

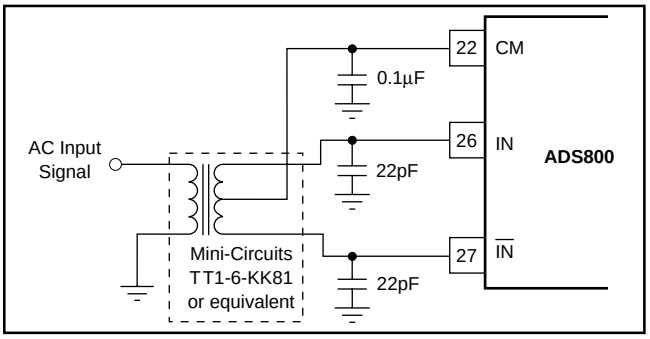


FIGURE 5. AC-Coupled Single-Ended to Differential Drive Circuit Using a Transformer.

Capacitors C_{SH1} and C_{SH2} are used to minimize current glitches resulting from the switching in the input track-and-hold stage and to improve signal-to-noise performance. These capacitors can also be used to establish a low-pass filter and effectively reduce the noise bandwidth. In order to create a real pole, resistors R_{SER1} and R_{SER2} were added in series with each input. The cutoff frequency of the filter is determined by $f_C = 1/(2pR_{SER} \bullet (C_{SH} + C_{ADC}))$ where R_{SER} is the resistor in series with the input, C_{SH} is the external capacitor from the input to ground, and C_{ADC} is the internal input capacitance of the A/D converter (typically 4pF).

Resistors R_1 and R_2 are used to derive the necessary common-mode voltage from the buffered top and bottom references. The total load of the resistor string should be selected so that the current does not exceed 1mA. Although the circuit in Figure 6 uses two resistors of equal value so that the common-mode voltage is centered between the top and bottom reference (+2.25V), it is not necessary to do so. In all cases the center point, V_{CM}, should be bypassed to ground in order to provide a low-impedance AC ground.

If the signal needs to be DC coupled to the input of the ADS800, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be accomplished by

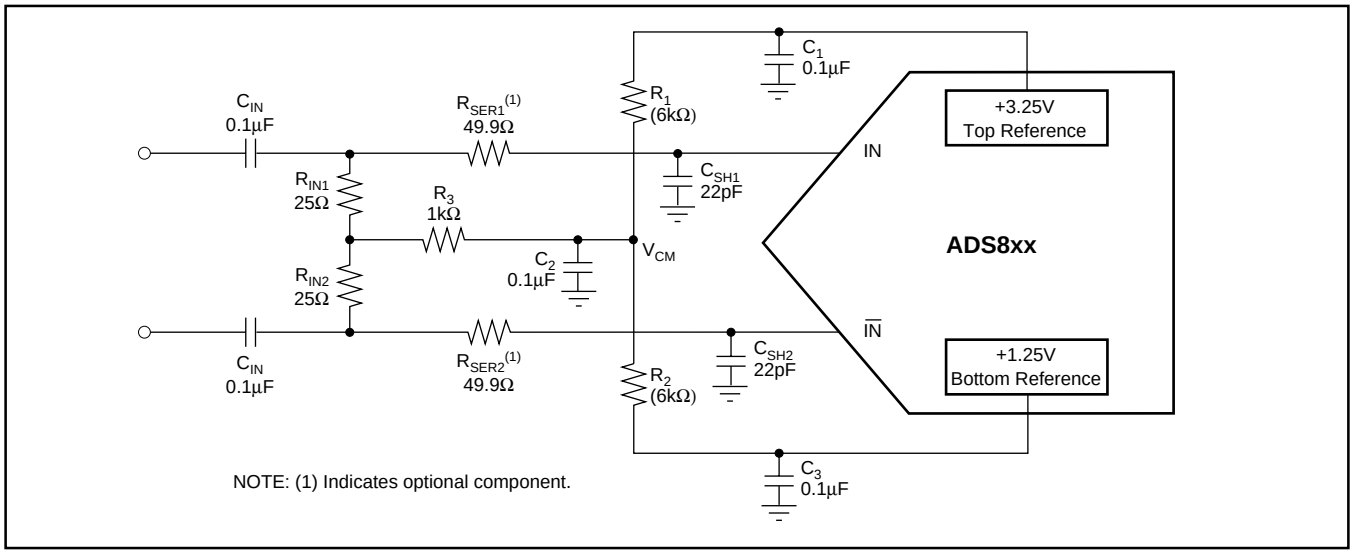


FIGURE 6. AC-Coupled Differential Input Circuit.

using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low distortion circuit in Figure 7 will provide the necessary input shifting required for signals centered around ground. It also employs a diode for output level shifting to ensure a low distortion +3.25V output swing. Other amplifiers can be used in place of the OPA842s if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a ±5V supply operational amplifier.

The ADS800 can also be configured with a single-ended input full-scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage, as shown in Figure 8. This configuration will result in increased even-order harmonics, especially at higher input frequencies. However, this tradeoff may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

EXTERNAL REFERENCES AND ADJUSTMENT OF FULL-SCALE RANGE

The internal reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may be overridden by external references that have at least 18mA (at room temperature) of output drive capability. In this instance, the common-mode voltage will be

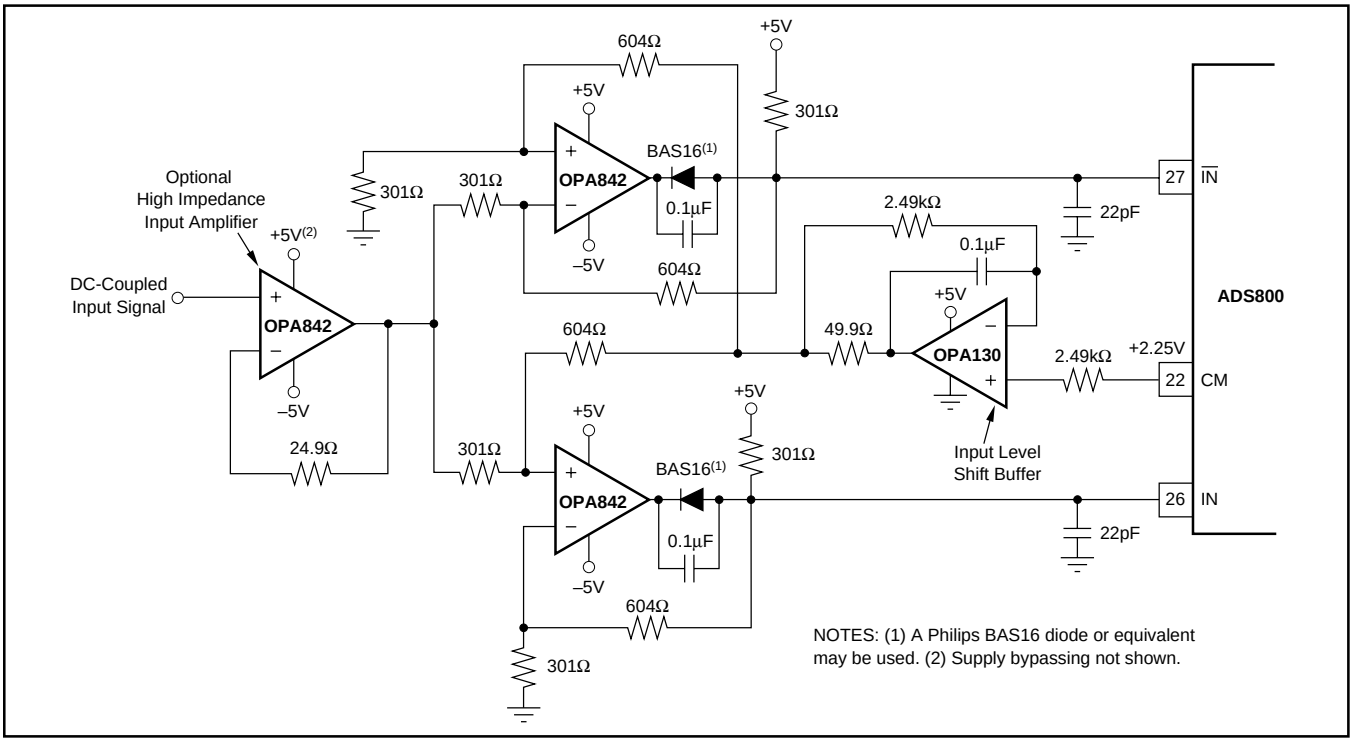


FIGURE 7. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

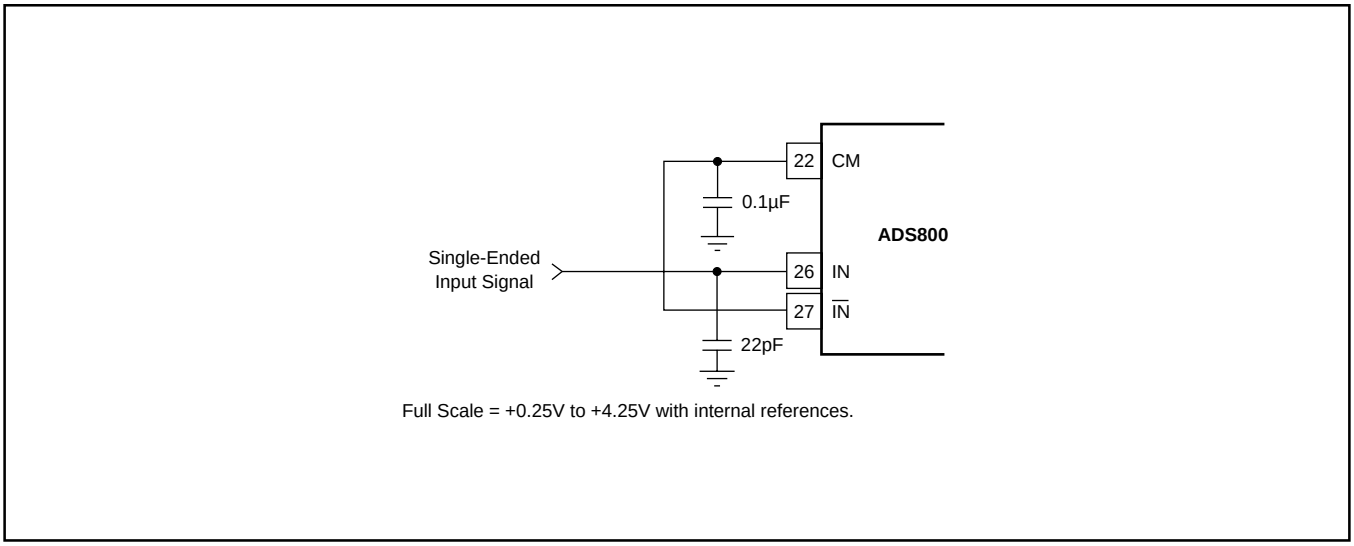


FIGURE 8. Single-Ended Input Connection.

set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full-scale input range of the ADS800. Changing the full-scale range to a lower value has the benefit of easing the swing requirements of external input drive amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V, the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V, and the difference between the external references are greater than or equal to 1.5V.

For the differential configuration, the full-scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is 2 • ($REFT_{EXT}$ – $REFB_{EXT}$), with the common-mode being centered at ($REFT_{EXT}$ + $REFB_{EXT}$)/2. Refer to the typical characteristics for “Expected Performance vs Full-Scale Input Range”.

The circuit in Figure 10 works completely on a single +5V supply. As a reference element, it uses the micro-power reference REF1004-2.5, which is set to a quiescent current of 0.1mA. Amplifier A_2 is configured as a follower to buffer the +1.25V generated from the resistor divider. To provide the necessary current drive, a pull-down resistor, R_P, is added.

Amplifier A_1 is configured as an adjustable gain stage, with a range of approximately 1 to 1.32. The pull-up resistor again relieves the op amp from providing the full current drive. The value of the pull-up/down resistors is not critical and can be varied to optimize power consumption. The need for pull-up, pull-down resistors depends only on the drive capability of the selected drive amplifiers and thus can be omitted.

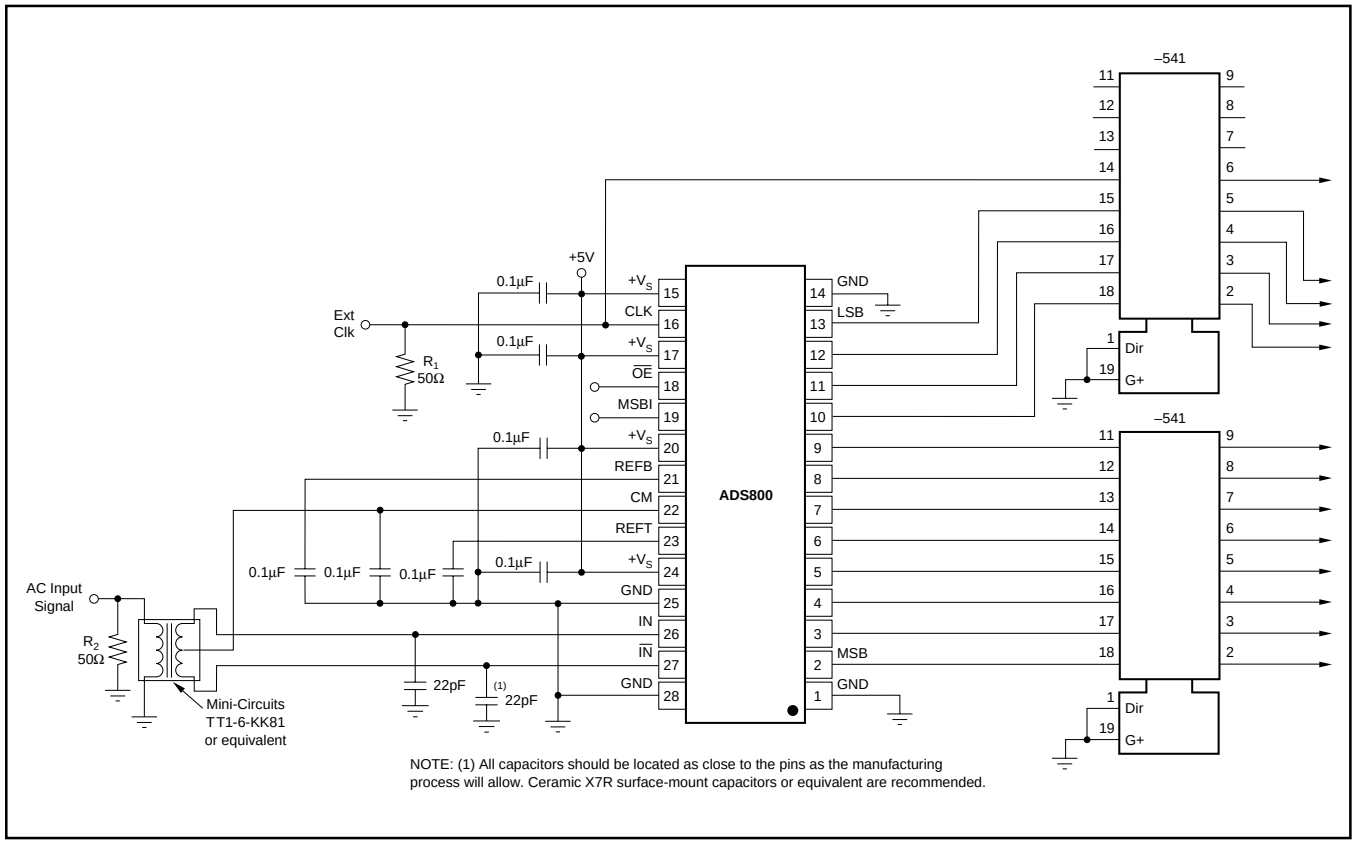


FIGURE 9. ADS800 Interface Schematic with AC-Coupling and External Buffers.

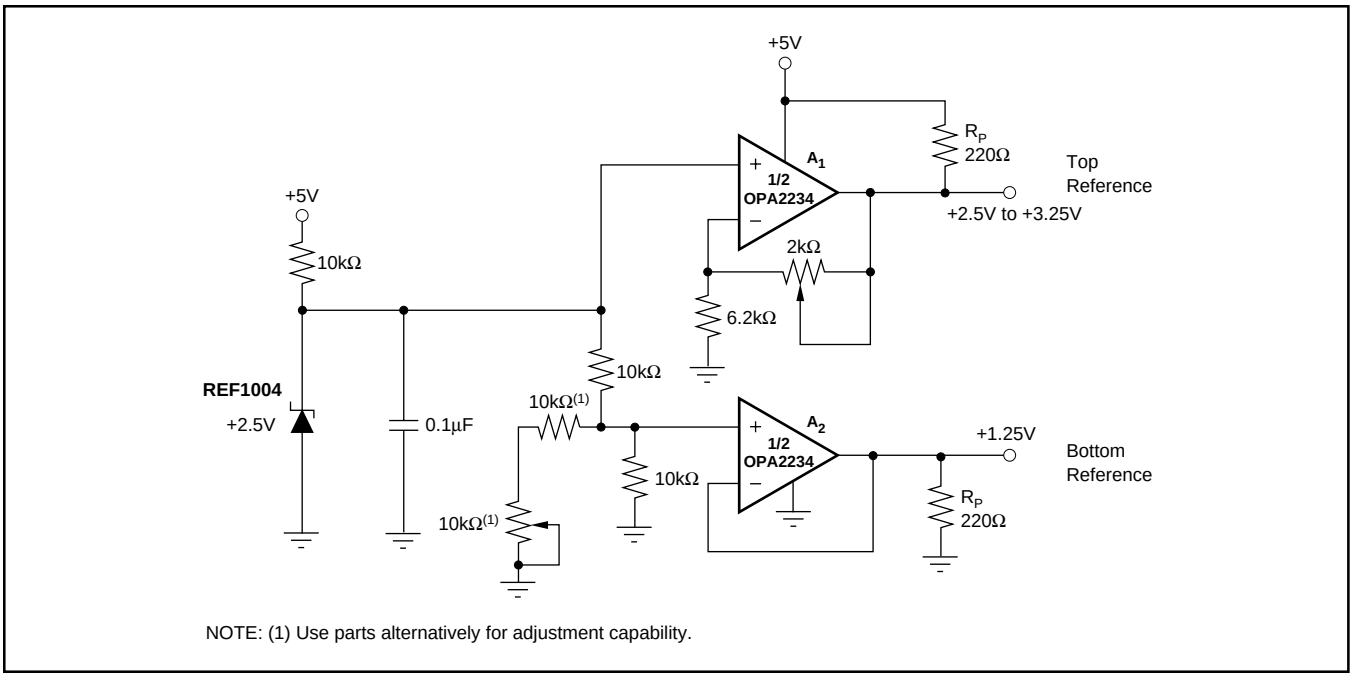


FIGURE 10. Optional External Reference to Set the Full-Scale Range Utilizing a Dual, Single-Supply Op Amp.

PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high-frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS800 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D converter power-supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS800 is a high performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D converter clock, gives excellent results. Low-pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS800. Using a signal amplitude slightly lower than full-scale will allow a small amount of “headroom” so that noise or DC offset voltage will not over-range the A/D converter and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise} + \text{Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th} - \text{order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals, f_1 or f_2. Five “bins” either side of peak are used for calculation of fundamental and harmonic power. The “0” frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.